

BANDON/NorthBay 13" Schematics Document

Whiskey Lake -U 42

2019-02-12

REV:A00

DY : None Installed
WWAN:For WWAN installed
LAN:For LAN Installed
Sensor:For Sensor Installed
Debug:For Debug Port installed

<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

Bandon / NorthBay 13"

Rev
X00

Date: Friday, February 15, 2019

Sheet 1 of 106

Project code : 4PD0G3010001
PCB P/N : 18717
Revision : -1

Lat Function	R45/Transformer	Bandon	NorthBay
LAN IC	De-pop	Pop	De-pop
E-compass	Pop	De-pop	Pop
Accelerometer + Gyro	Pop	De-pop	Pop
P-sensor	Pop	De-pop	Pop
Led	Pop	De-pop	Pop
Hall sensor	Pop	De-pop	Pop

eDP 13" Panel
55

Touch Panel
55

Intel CPU
WHISKEY LAKE-U 42
WHL U PCH-LP
16 PCIe* Lanes
3 SATA Lanes
6 USB3.1 Gen1/Gen2 Lanes
5 GbE Lanes
2 Remapped PCIe* storage

DDR4 Channel A
DDR4 2400
SODIMM A
12

DDR4 Channel B
DDR4 2400
SODIMM B
13

USB PowerShare
SILEGO
SLGC55544CVTR
36

Bandon/Northbay 13" Block Diagram

NON-INTERLEAVE MODE

USB3.1 / PowerShare
USB Port : 2
35

USB3.1
USB Port : 1
35

Internal Digital MIC
Camera
55

Universal Jack

(2W, 4ohm /channel)
2CH Speaker

Flash ROM
Winbond
W25Q64JVEIQ (64MB) non-Vpro SRU
W25Q256JVEIQ (32MB) Vpro SRU
25

Flash ROM
Winbond
W25Q128JVEIQ (128MB) non-Vpro
25

TPM 2.0
ST
ST33TPHF2XSPI
[Co-lay Nuvoton 750]
91

EC
SMSC
MEC 5106
24

KB/TP Conn
65

Thermal & Fan
26

eSPI debug port
68

Hall sensor
BANDON NORTHBAY
TCS40DLR APX8131A
67

LED BD
64

Finger Printer
92

CV3 Lynx Controller
Broadcom
BCM58202
66

FLASH ROM
SOP8 6*5
Winbond
MX25L12872FM2I (16MB)
RFID/NFC
RFID Antenna

SmartCard IC
NXP
TDA8034HN
Connector
Smart Card

Accelerometer
ST
LNG2DMTR
70

E-compass
ST
LIS2MDLTR
70

Accelerometer + Gyro
ST
LSM6DSUSTR
70

P-sensor
SEMTECH
SX9310
70

Charger		44
ISL9538HRTZ-GP-U		
INPUTS	OUTPUTS	
BT+	DCBATOUT	
SYSTEM DC/DC		45
SY8288BRAC/SY8288CRAC		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5	
	3D3V_S5	
	5V_AUX_S5	
	5V_S5	
CPU DC/DC		47
FDMF3035-GP		
INPUTS	OUTPUTS	
DCBATOUT	1V_VCCGT	
CPU DC/DC		50
ISL95808HRZ-T-1-GP		
INPUTS	OUTPUTS	
DCBATOUT	1V_VCCSA	
SYSTEM DC/DC		51
SY8288RAC		
INPUTS	OUTPUTS	
DCBATOUT	1D2V_S3	
SYSTEM DC/DC		52
AOZ2260QI-10-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S5	
SYSTEM DC/DC		54
RT6542AGQW-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_VCCPRIM_CORE	
Load Switches		
INPUTS	OUTPUTS	
3D3V_S5	3D3V_S5_PCH	
	3D3V_LAN	
	3D3V_S5_WWAN	
	3D3V_S5_WLAN	
	2D5V_S3	
	1D8V_S5	
	VCDVDD_FUSE	
	3D3V_S0	
3D3V_S0	+3V_AVDD	
	3D3V_CAMERA_S0	
	3D3V_S0_SATA	
5V_S5	5V_S0	
	1D05V_VCCIO	
5V_S0	+5V_PVDD	
	5V_TSP_S0	
	5V_HDMI	
1D8V_S5	1D8V_S0	
1D2V_S3	0D6V_S0	
	1D2V_VCCPLL_OC	
1D05V_S5	1D05V_VCCSTG	
	1D05V_VCCSTG	
PCB LAYER (FR4-10 Layer)		
L1: Top	L6: Signal	
L2: GND	L7: GND/PWR	
L3: Signal	L8: Signal	
L4: GND	L9: GND	
L5: Signal	L10: Bottom	

Core Design

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Block Diagram	
File	
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Main Func = CPU

[24]	PECI_CPU	<< >>
[24,43,44,46]	PROCHOT#_CPU	<< >>
[24]	THERMTRIP#_CPU	<< >>
[99]	BPM_N0	<<< >>>
[99]	BPM_N1	<<< >>>
[99]	CPU_JTAG_TCK	<< >>
[99]	CPU_JTAG_TDI	<< >>
[99]	CPU_JTAG_TDO	<< >>
[99]	CPU_JTAG_TMS	<< >>
[99]	CPU_JTAG_TRST#	<< >>
[99]	CPU_JTAG_PRDY#	<< >>
[99]	CPU_JTAG_PREQ#	<< >>
[99]	PCH_JTAG_TCK	<< >>
[17]	H_CUPWRGD	>> >>
[55]	TOUCH_SCREEN_PD#_R	>> >>
[24,65]	TOUCHPAD_INTR#	>> >>
[55]	TOUCH_SCREEN_DET#	>> >>

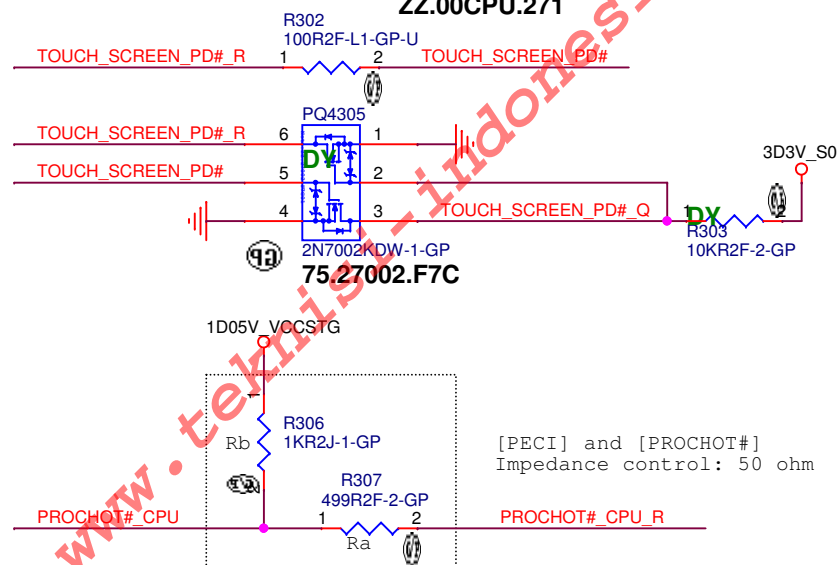
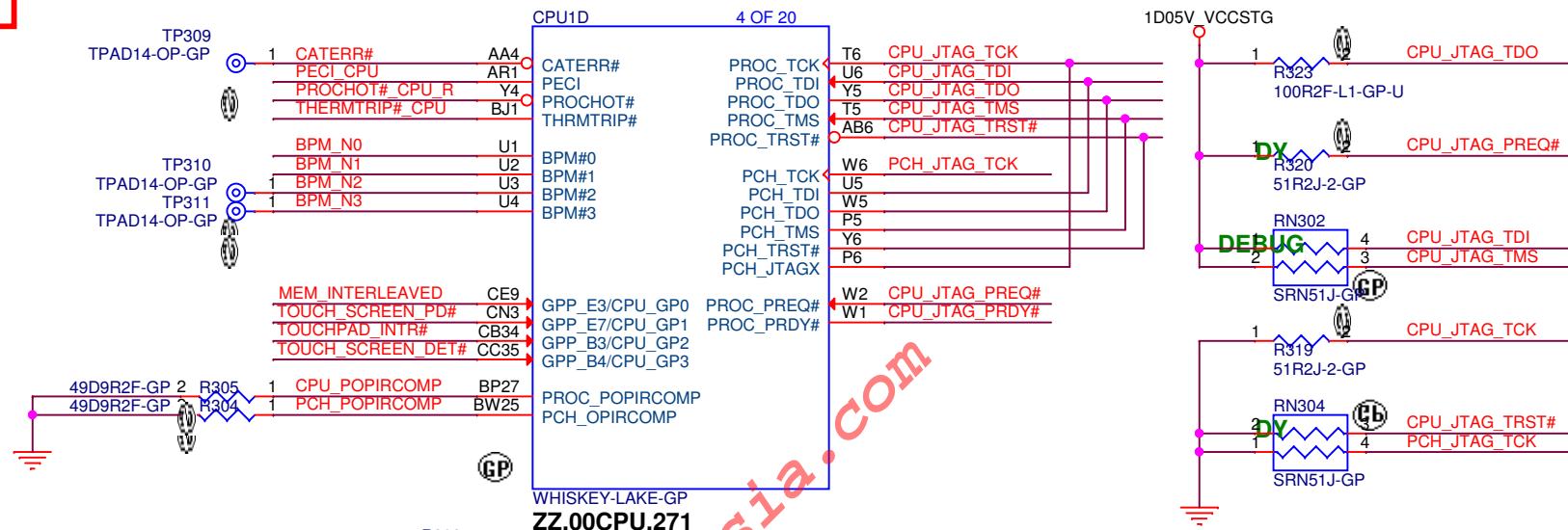
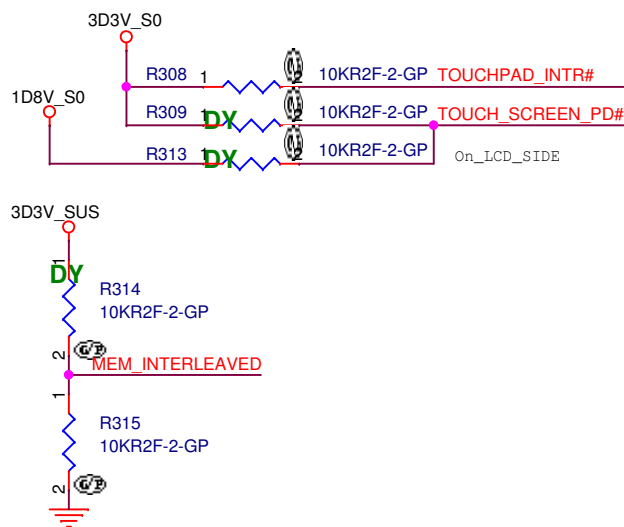
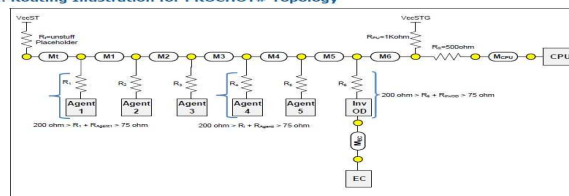


Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

DIMM_TYPE	
LOW	HIGH
NON_INTERLEAVED	INTERLEAVED

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Main Func = CPU

Edp

[55] eDP_TX_CPU_N0 <<<
[55] eDP_TX_CPU_P0 <<<
[55] eDP_TX_CPU_N1 <<<
[55] eDP_TX_CPU_P1 <<<

[55] eDP_AUX_CPU_N <<<
[55] eDP_AUX_CPU_P <<<

[55] EDP_HPD >>>

[55] eDP_BLEN_CPU <<<
[55] eDP_BLCTRL_CPU <<<
[55] eDP_VDDEN_CPU <<<

DP to AR

[71] DP_DDI_TX_N0 <<<
[71] DP_DDI_TX_P0 <<<
[71] DP_DDI_TX_N1 <<<
[71] DP_DDI_TX_P1 <<<
[71] DP_DDI_TX_N2 <<<
[71] DP_DDI_TX_P2 <<<
[71] DP_DDI_TX_N3 <<<
[71] DP_DDI_TX_P3 <<<

[71] DP_AUX_CPU_N <<<
[71] DP_AUX_CPU_P <<<

[71] DP_HPD_CPU >>>

[71] CPU_DP_CTRL_DATA <<<
[71] CPU_DP_CTRL_CLK <<<

DP to AR

[71] DP2_DDI_TX_N0 <<<
[71] DP2_DDI_TX_P0 <<<
[71] DP2_DDI_TX_N1 <<<
[71] DP2_DDI_TX_P1 <<<
[71] DP2_DDI_TX_N2 <<<
[71] DP2_DDI_TX_P2 <<<
[71] DP2_DDI_TX_N3 <<<
[71] DP2_DDI_TX_P3 <<<

[71] DP2_AUX_CPU_P <<<
[71] DP2_AUX_CPU_N <<<

[71] DP2_HPD_CPU <<<

DP to AR

DP_DDI_TX_N0 AL5
DP_DDI_TX_P0 AL6
DP_DDI_TX_N1 AJ5
DP_DDI_TX_P1 AJ6
DP_DDI_TX_N2 AF6
DP_DDI_TX_P2 AF5
DP_DDI_TX_N3 AE5
DP_DDI_TX_P3 AE6

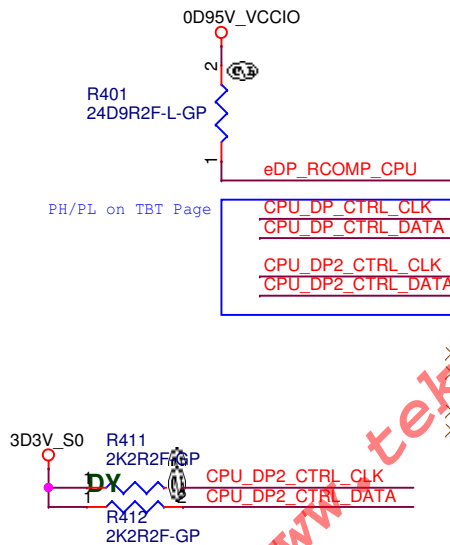
DP to AR

DP2_DDI_TX_N0 AC4
DP2_DDI_TX_P0 AC3
DP2_DDI_TX_N1 AC1
DP2_DDI_TX_P1 AC2
DP2_DDI_TX_N2 AE4
DP2_DDI_TX_P2 AE3
DP2_DDI_TX_N3 AE1
DP2_DDI_TX_P3 AE2

575412
eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length
eDP_RCOMP	5 mils	25 mils	24.9 or 100 Ω \pm 1%	600 mils

Note: Must maintain low DC resistance routing (<0.1 Ω)



		CPU (ITBT, DP1.4, USB3.1 g2)				
Canon Lake U PCH-LP		eDP DDI A	DDI 1	DDI 2		
North Bay 13 Bandon	13 UU (non-TBT)	LCD	HDMI 1.4	Type-C Port 1		
	13 UU (TBT)	LCD	TBT (Alpine Ridge Port 0)	TBT (Alpine Ridge Port 1)	HDMI on AR side-port	

CPU1A

DDI1_TXN0
DDI1_TXP0
DDI1_TXN1
DDI1_TXP1
DDI1_TXN2
DDI1_TXP2
DDI1_TXN3
DDI1_TXP3

DDI2_TXN0
DDI2_TXP0
DDI2_TXN1
DDI2_TXP1
DDI2_TXN2
DDI2_TXP2
DDI2_TXN3
DDI2_TXP3

1 OF 20

EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1
EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3

EDP_AUX_N
EDP_AUX_P

DISP_UTILS

DDI1_AUX_N
DDI1_AUX_P
DDI2_AUX_N
DDI2_AUX_P
DDI3_AUX_N
DDI3_AUX_P

GPP_E13/DDPB_HPD0/DISP_MISC0
GPP_E14/DDPC_HPD1/DISP_MISC1
GPP_E15/DPPD_HPD2/DISP_MISC2
GPP_E16/DPPD_HPD3/DISP_MISC3
GPP_E17/EDP_HPD/DISP_MISC4

EDP_BKLTEN
EDP_VDDEN
EDP_BKLCTCL

DISP_RCOMP

GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
GPP_E19/DPPB_CTRLCLK

GPP_E20/DPPC_CTRLCLK
GPP_E21/DPPC_CTRLCLK

GPP_E22/DPPD_CTRLCLK
GPP_E23/DPPD_CTRLCLK

GPP_H16/DDPF_CTRLCLK
GPP_H17/DDPF_CTRLCLK

WHISKEY-LAKE-GP

ZZ.00CPU.271

AG4 eDP_TX_CPU_N0
AG3 eDP_TX_CPU_P0
AG2 eDP_TX_CPU_N1
AG1 eDP_TX_CPU_P1
AJ4
AJ3
AJ2
AJ1

AH4 eDP_AUX_CPU_N
AH3 eDP_AUX_CPU_P

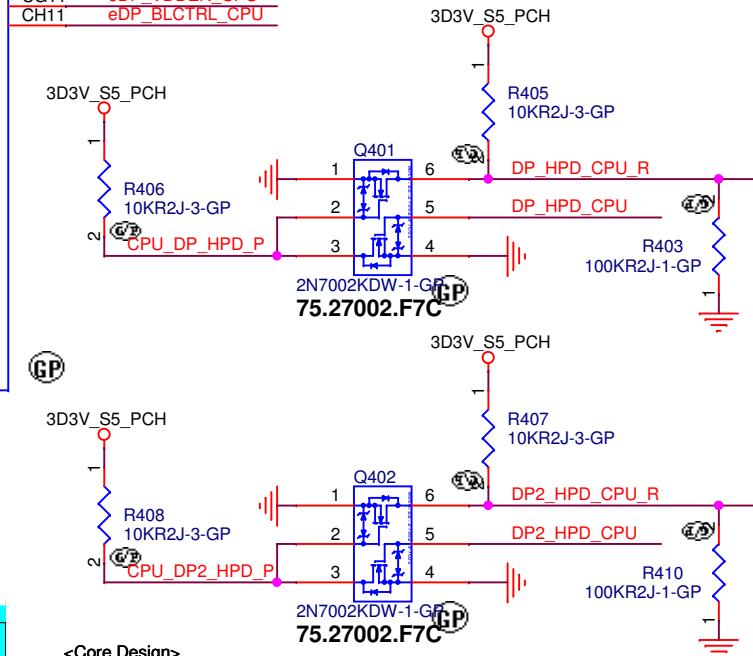
AM7
AC7 DP_AUX_CPU_N
AC6 DP_AUX_CPU_P
AD4 DP2_AUX_CPU_N
AD3 DP2_AUX_CPU_P

AG7
AG6

CN6 DP_HPD_CPU_R
CM6 DP2_HPD_CPU_R
CP7
CP6 FFS_INT2
CM7 EDP_HPD

CK11 eDP_BLEN_CPU
CG11 eDP_VDDEN_CPU
CH11 eDP_BLCTRL_CPU

For AR



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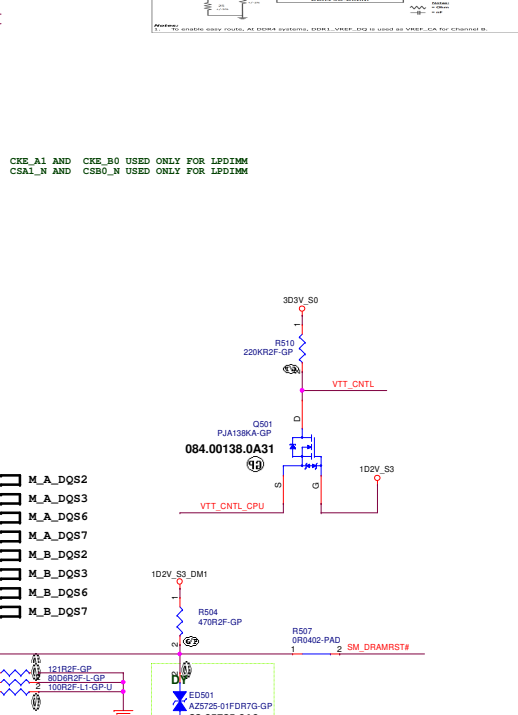
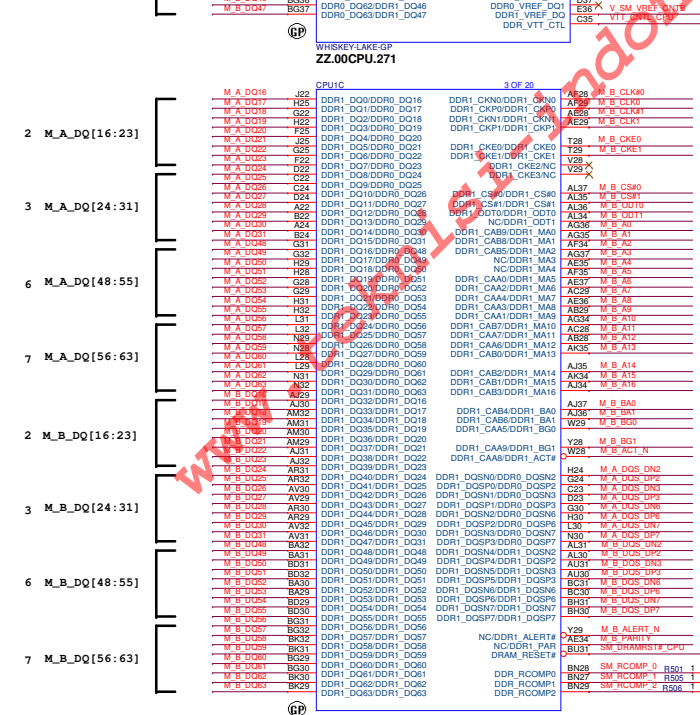
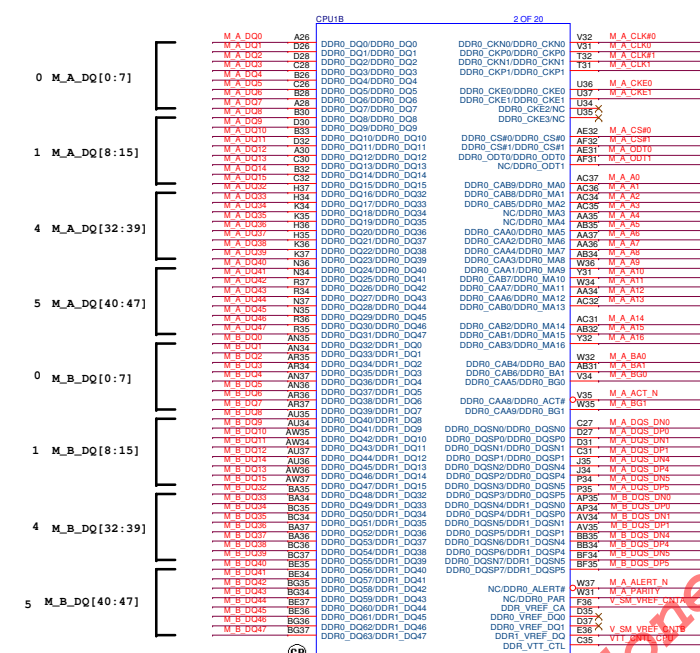
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Title CPU_(JTAG/CPU SIDE BAND)

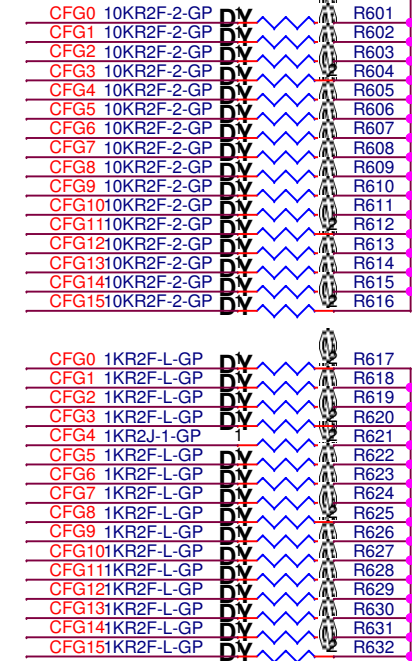
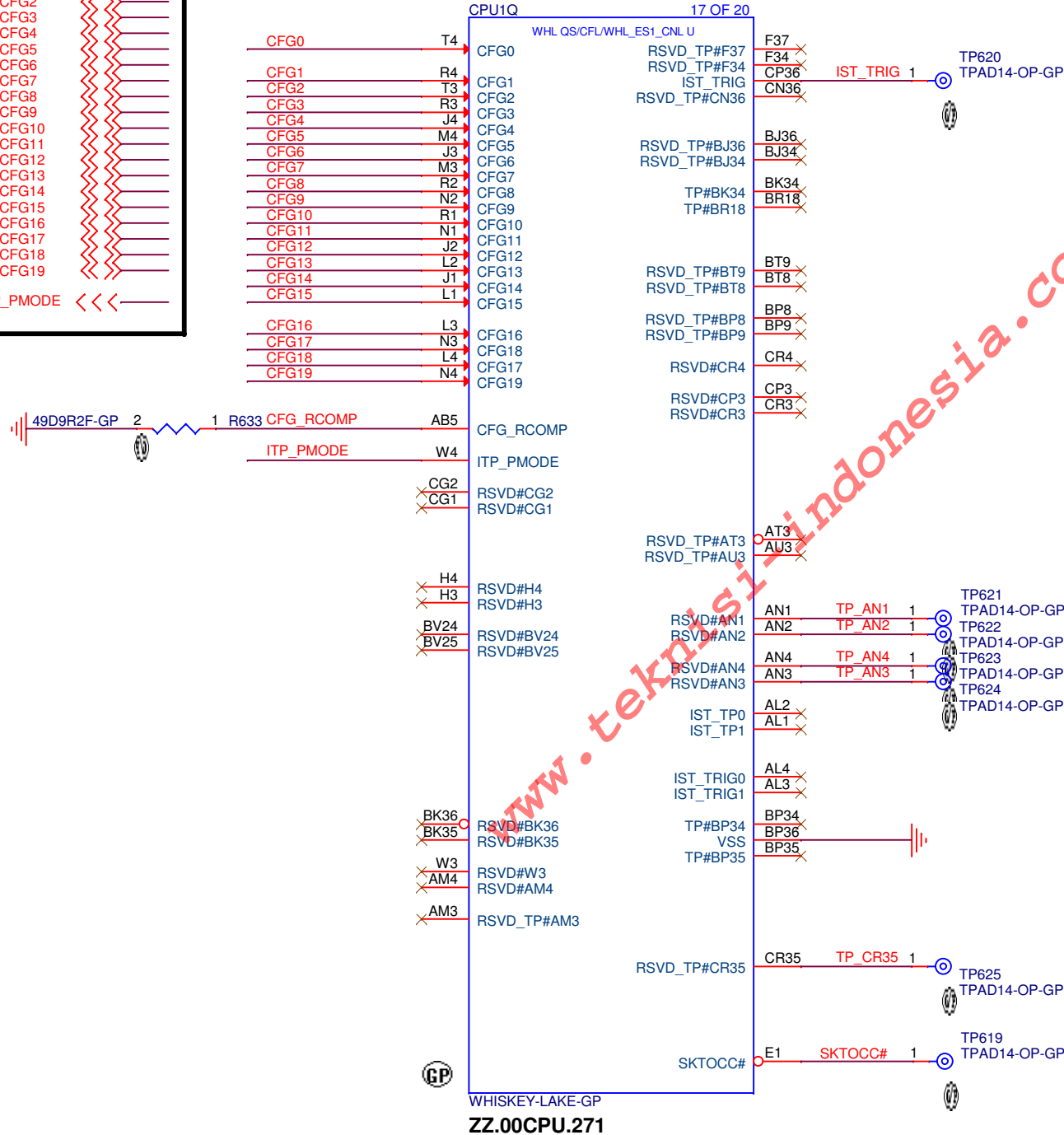
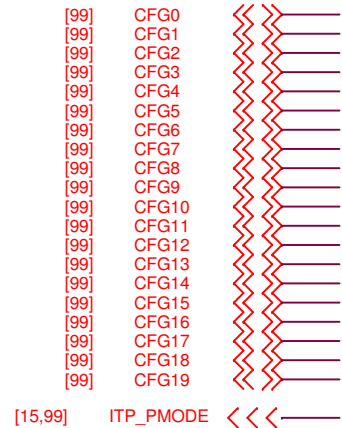
Size A4 Document Number Bandon / NorthBay 13" Rev X00

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DDR4 ball type: NON- Interleaved Type



Main Func = CPU



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Title

CPU (RESERVED)

Size
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Document Number

Bandon / NorthBay 13"

Rev
X00

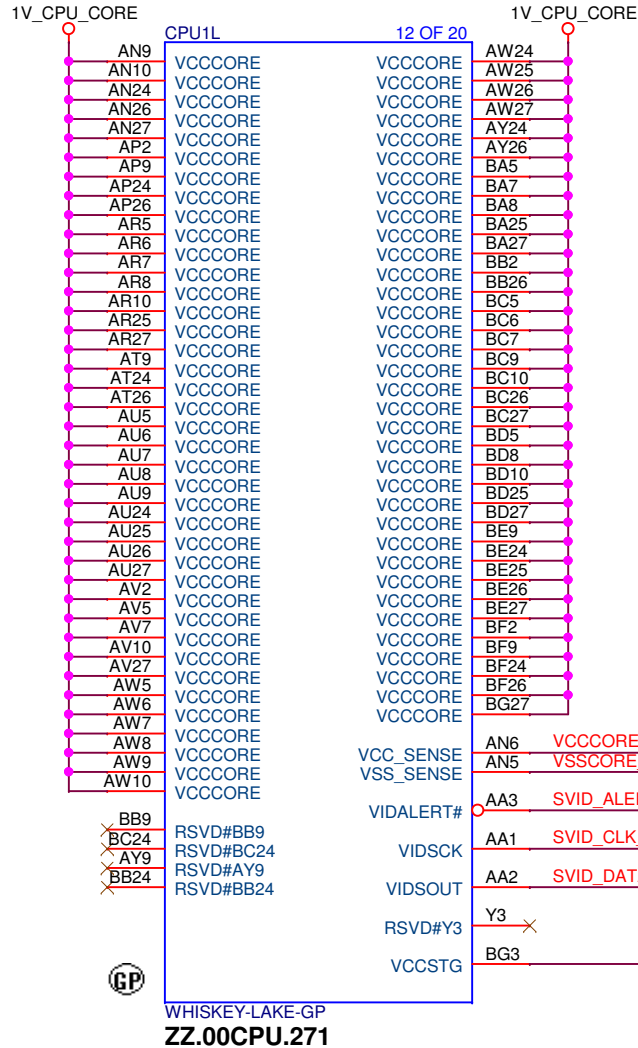
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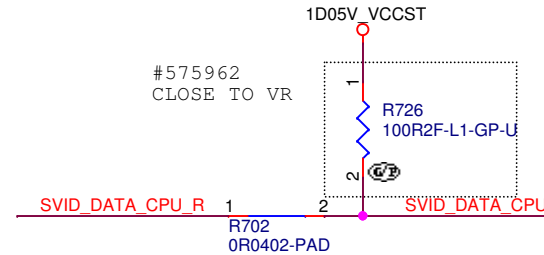
Main Func = CPU

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
Route the Alert signal between the Clock and the Data signals.

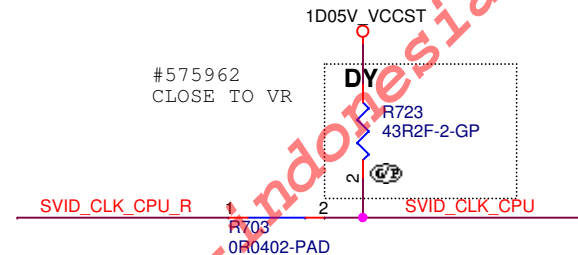
[46] VCCCORE_SENSE <<<<
[46] VSSCORE_SENSE <<<<
[46] SVID_DATA_CPU <<<<
[46] SVID_CLK_CPU <<<<
[46] SVID_ALERT#_CPU <<<<



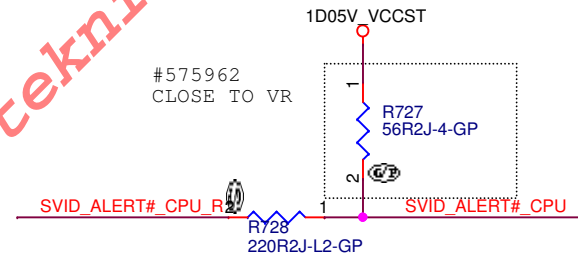
SVID DATA



SVID CLOCK



SVID ALERT



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

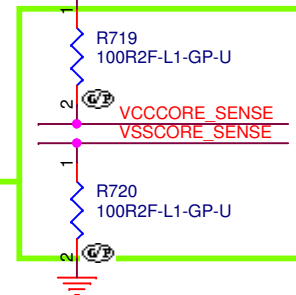
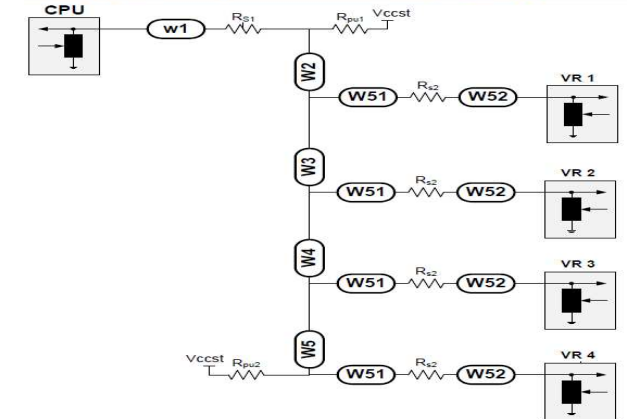


Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W1 [inches]	W2 [inches]	R _{bus} [Ω]	R _{bus} [Ω]	R _{bus} [Ω]	R _{bus} [Ω]	W _{CPU} [inches]
VIDSOUT							100	100	0	10	
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDALERT #							56	Empty	220	0	

Figure 10-7. Routing Illustration for SVID Topology



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CPU(VCC CORE)

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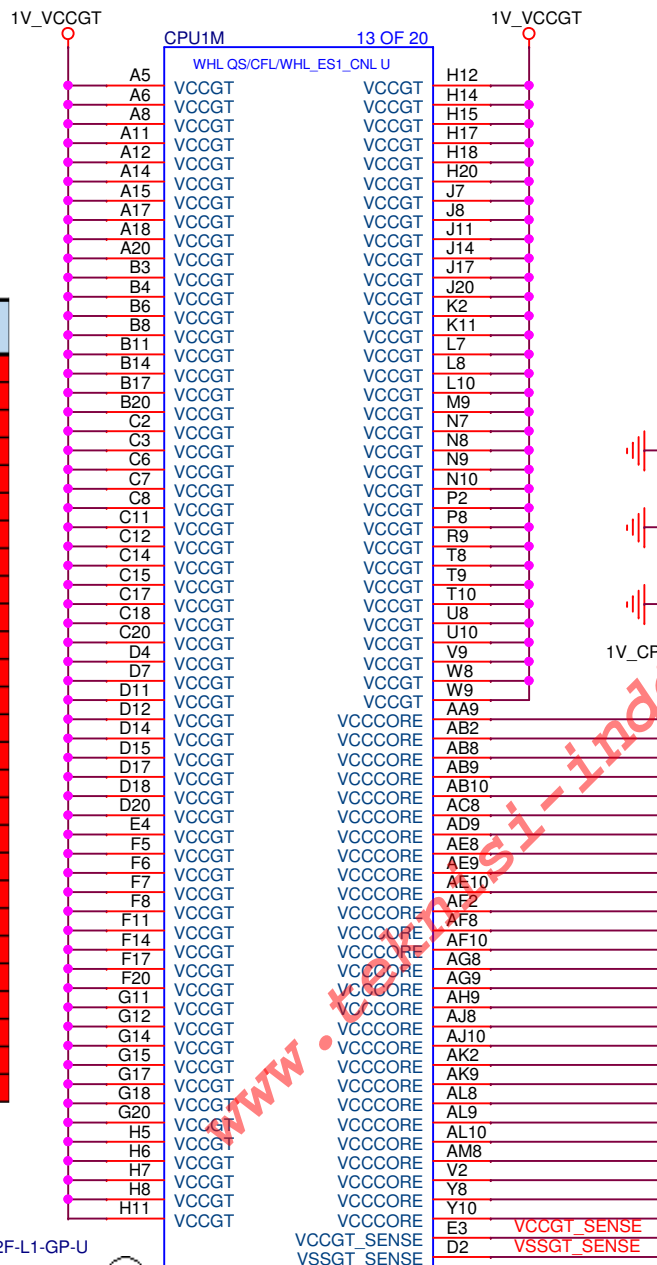
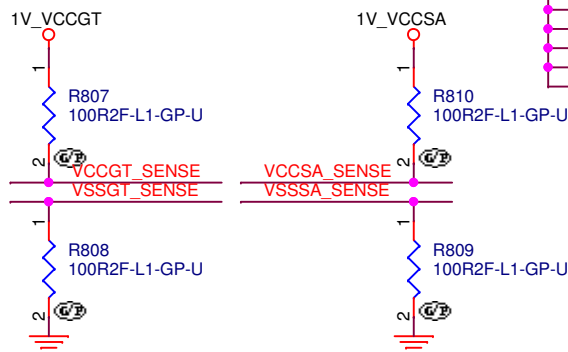
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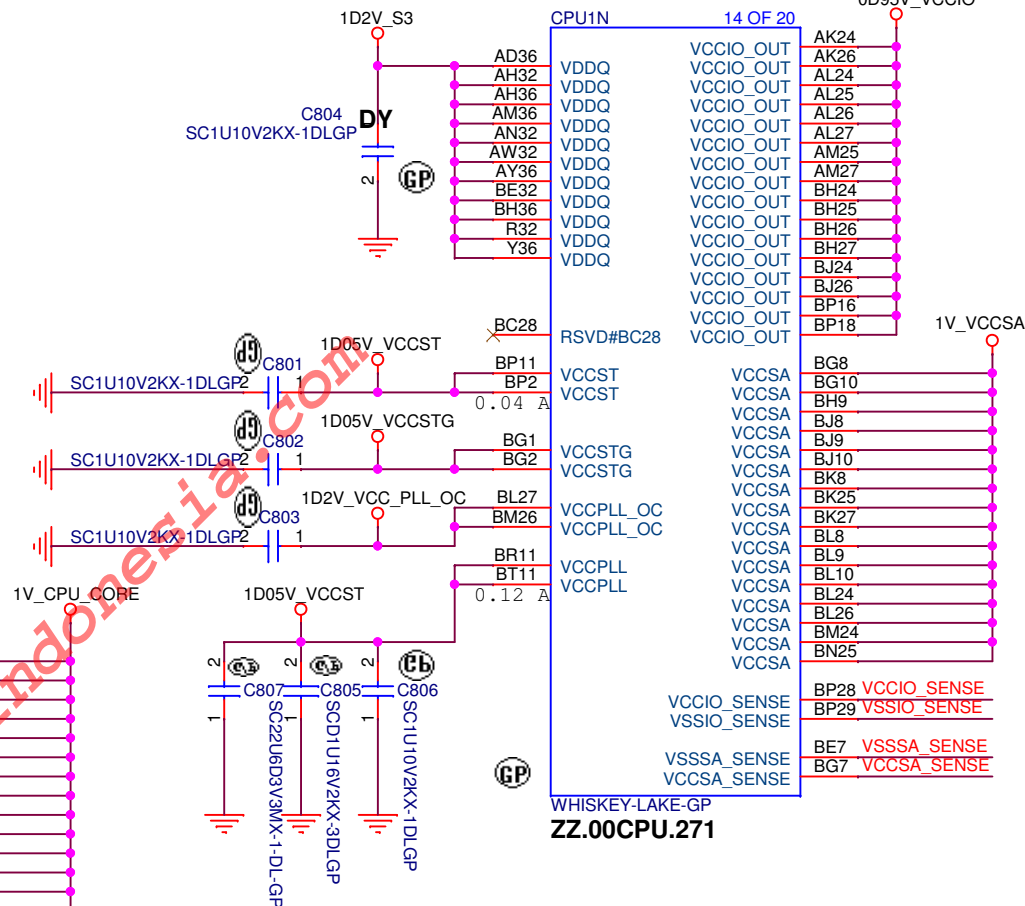
Main Func = CPU

[46] VCCGT_SENSE <<<< —
[46] VSSGT_SENSE <<<< —
[46] VSSA_SENSE <<<< —
[46] VCCA_SENSE <<<< —
[54] VCCIO_SENSE >>>> —
[54] VSSIO_SENSE >>>> —

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



WHISKEY-LAKE-GP
ZZ.00CPU.271



WHISKEY-LAKE-GP
ZZ.00CPU.271

VCCPLL_OC	1x 1uF 0402		Do not merge VccPLL, VccPLL_OC and VccST to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
VccPLL	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		Placeholder Only. Can be placed on as either Primary or back side cap.
VccST	1x 1uF 0402		
VccSTG	1x 1uF 0402		

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Title			CPU (DISPLAY)	
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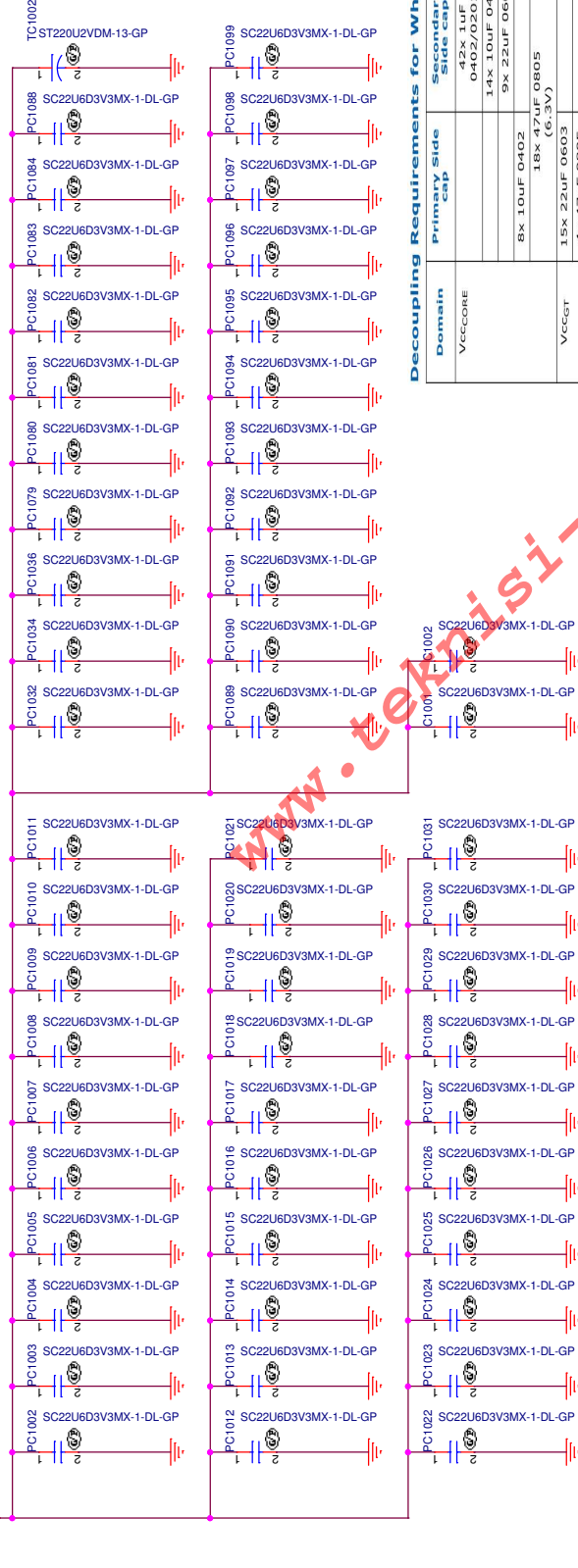
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Follow RO13 CAP account and vaule :

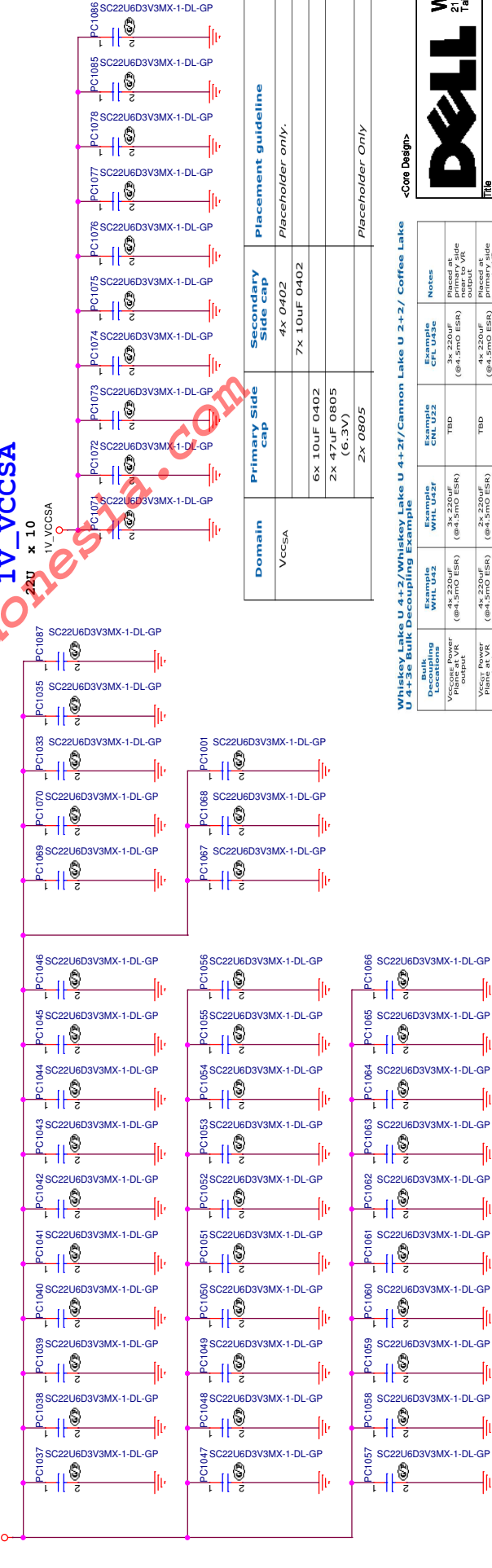
1V_CPU_CORE

22U*52/220U*1
1V_CPU_CORE



1V VCCGT

22U x 38
1V VCCGT



Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)			
Domain	Primary Side cap	Secondary Side cap	Placement guideline
V _{CCORE}		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
V _{CCGT}	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible.
	15x 22uF 0603		Can be placed on an either Primary or back side cap.
	4x 10uF 0805 (6.3V)		Place as close to the package as possible
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCSA		4x 0402	Placeholder only.
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		Placeholder Only

Whiskey Lake U 4+2/Whiskey Lake U 4+2f/Cannon Lake U 2+2/ Coffee Lake

	Bulk Decoupling Capacitor	VR Unit U22	VR Unit U23	VR Unit U24	VR Unit U25	VR Unit U26	Notes
Vccout Power output	4x 220µF (@±4.5mΩ ESR)	4x 220µF (@±4.5mΩ ESR)	3x 220µF (@±4.5mΩ ESR)	TBD	3x 220µF (@±4.5mΩ ESR)	Placed at primary side near VR output	
Vaux Power output	4x 220µF (@±4.5mΩ ESR)	4x 220µF (@±4.5mΩ ESR)	3x 220µF (@±4.5mΩ ESR)	TBD	4x 220µF (@±4.5mΩ ESR)	Placed at secondary side near VR output	

Notes:

1. Bulk capacitors are based on 10Hz switching frequency Vn with bandwidth of up to 250kHz.
2. Bandwidth Customers should work with respective vendor to validate their VR & bulk decoupling designs.

<Core Design>



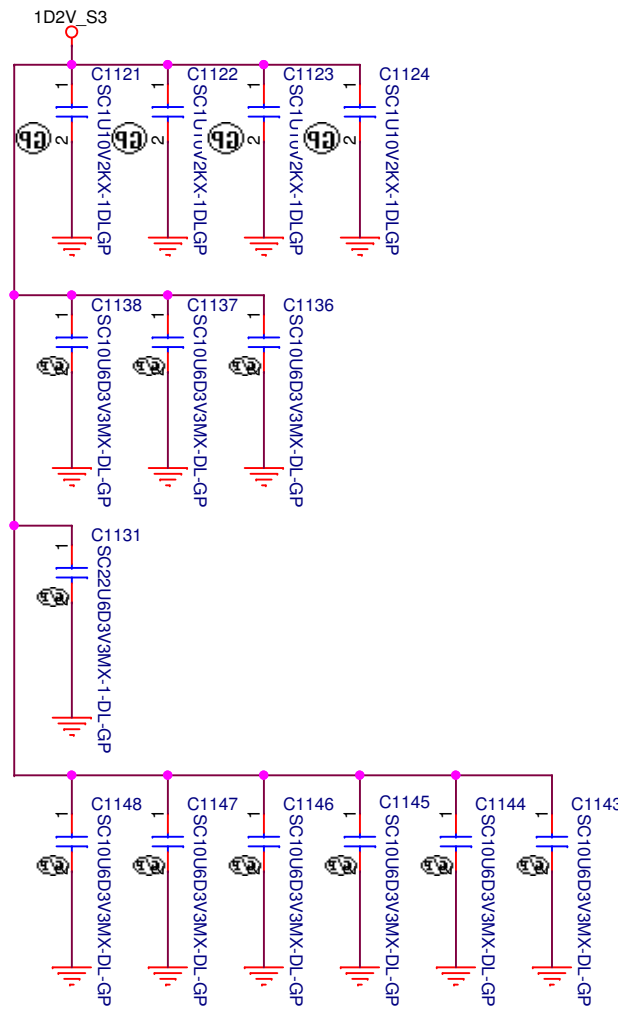
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CPU (Power CAP1)

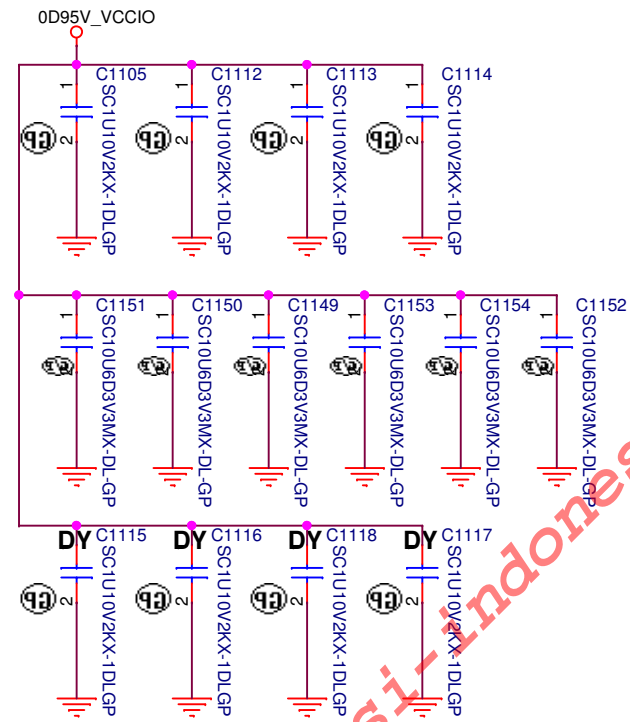
Size	Document Number	Rev
A3		X00
Bandon / NorthBay 13"		
Date: Friday, February 15, 2019	Sheet 10 of 106	

Main Func = CPU

VDDQ



VCCIO



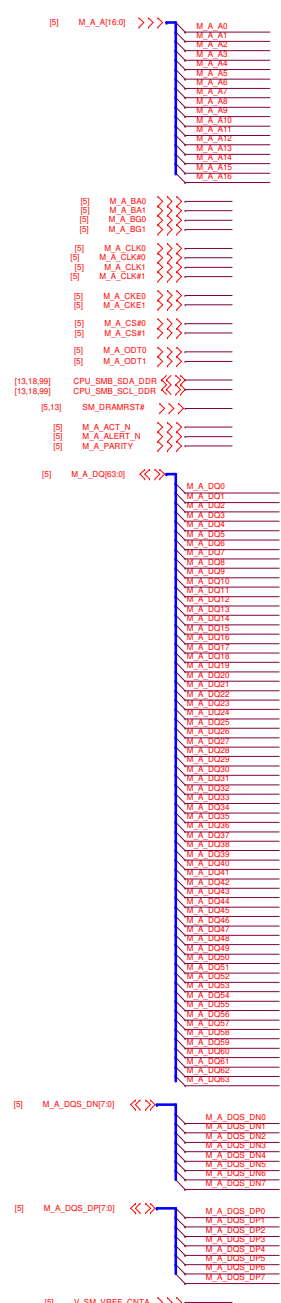
V _{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
V _{CCIO}	4x 1uF 0201		Place as close to the package as possible
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		Placeholder Only

<Core Design>

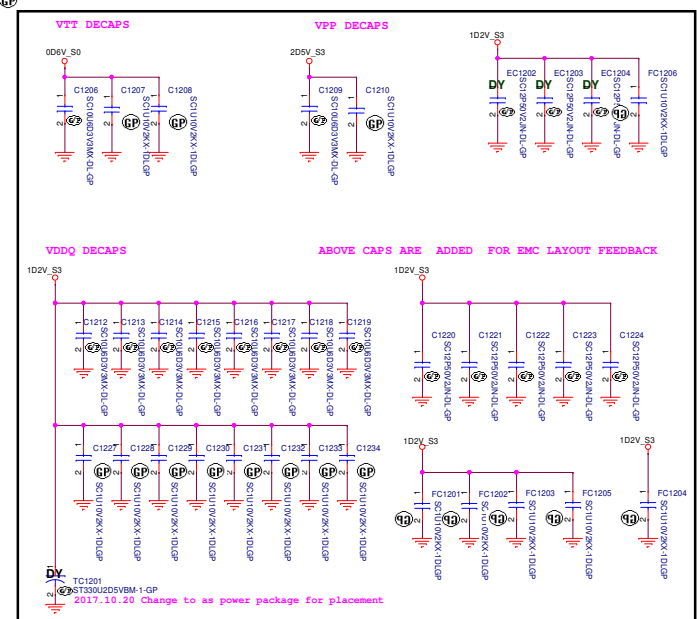
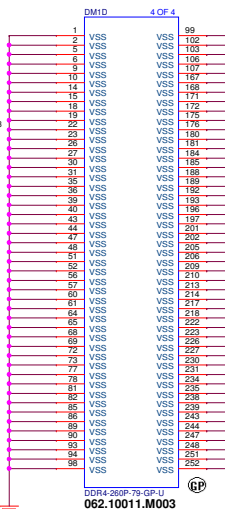
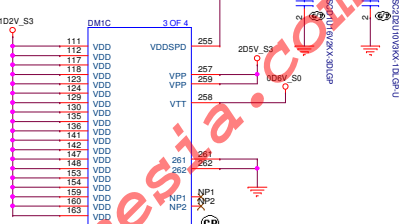
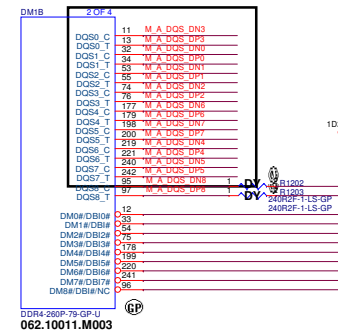
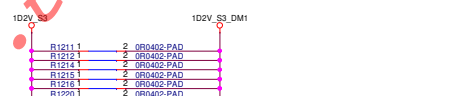
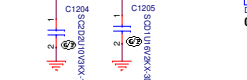
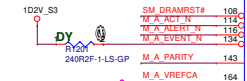
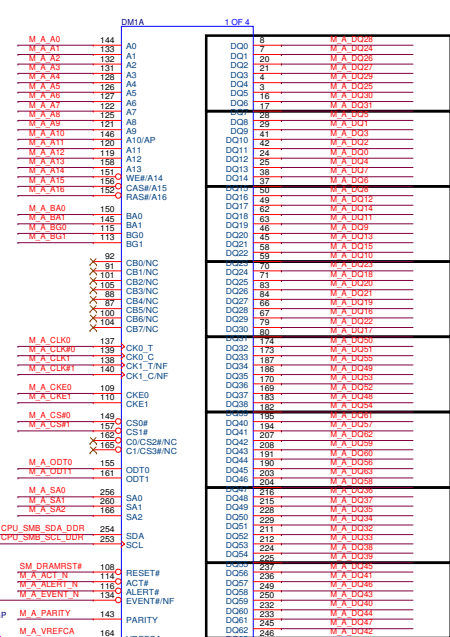


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Main Func = Memory



U0: Cap. Requirement: 100F (pin number) for reference use the data provided in the table. The capacitor value should be placed in the table.



WHL-U DDR4 SODIMM Decoupling

This recommendation assumes a 2CH, 1DPC (2 connector) implementation of SO-DIMMs.

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x uF (size)
DDR4 SODIMM 1DPC	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 10uF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1uF (0402)
	VTT	1 cap stuffed, 1 placeholder	2x 10uF (0603)
		Place on VTT plane close to SODIMM	4x 1uF (0402)
VPP	DIMM pin side, 1 per DIMM	DIMM pin side, 1 per DIMM	2x 10uF (0603)
		DIMM pin side, 1 per DIMM	2x 1uF (0402)
VDDSPD	Place close to DIMM	Place close to DIMM	2x 0.1uF (0402)
		Place close to DIMM	2x 2.2uF (0402)

Notes: 1. Total quantity is referring to 2 channels.

•Core Design•

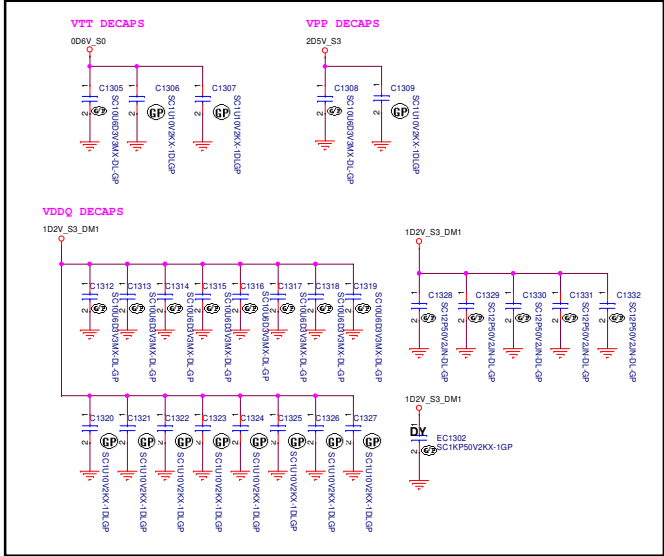
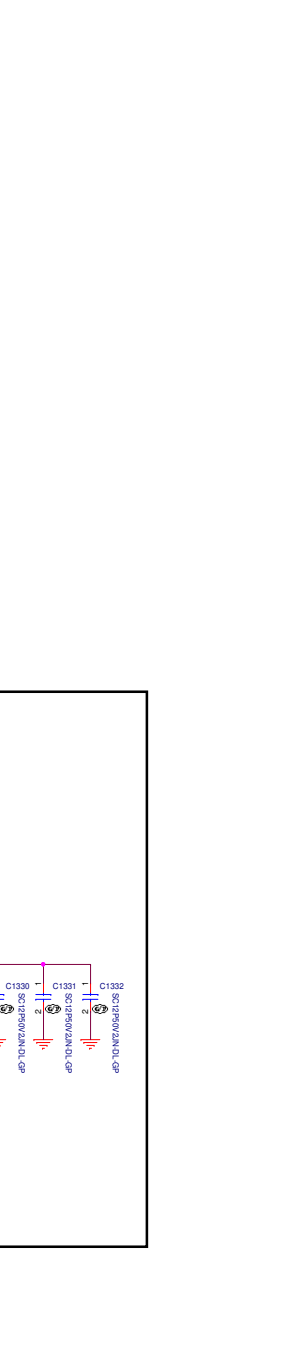
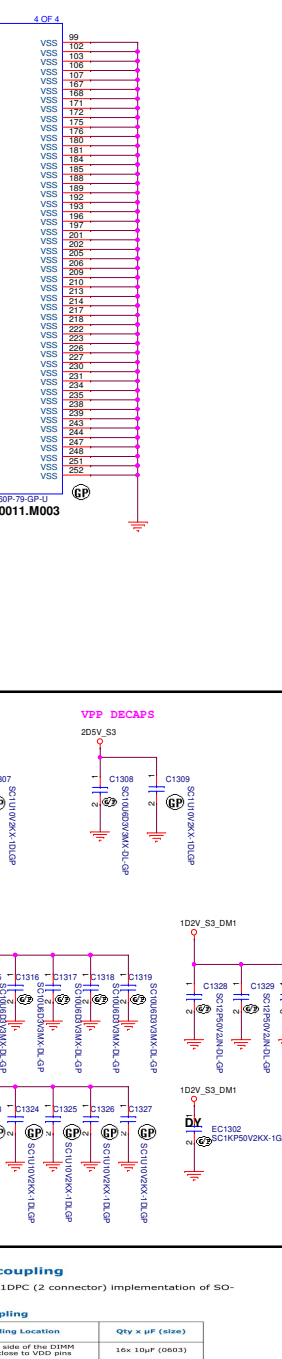
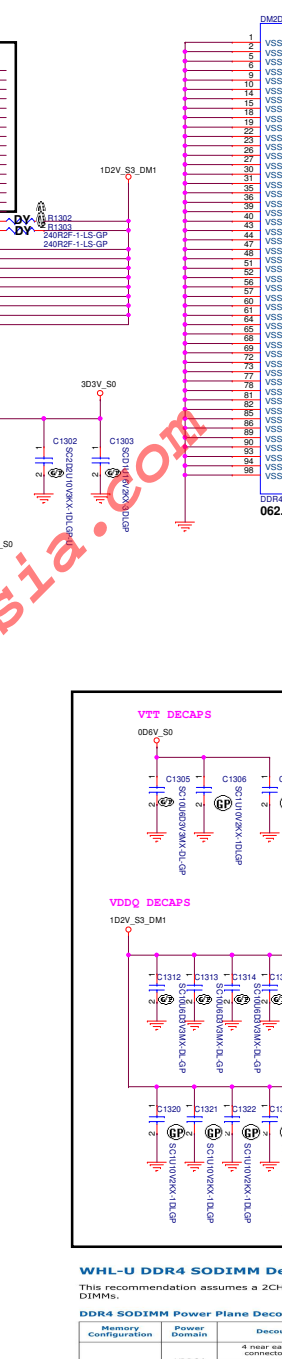
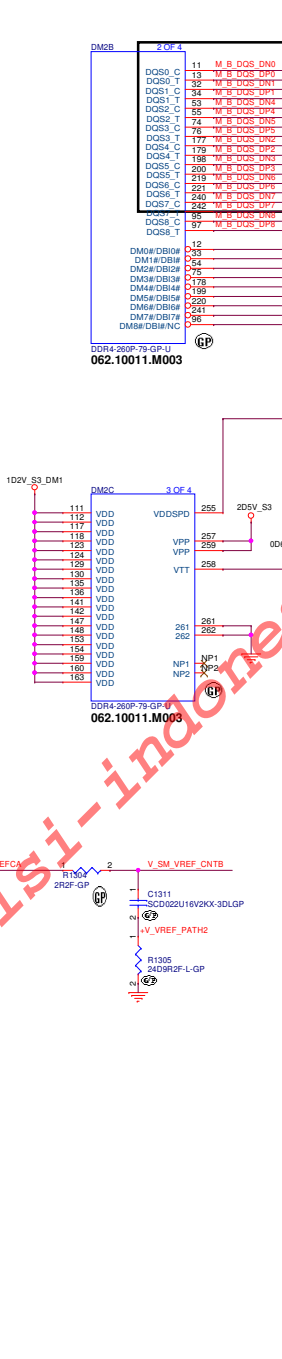
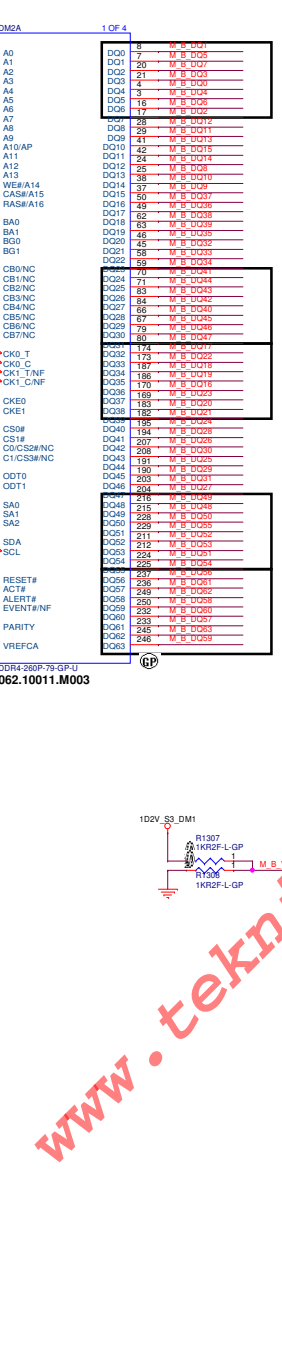
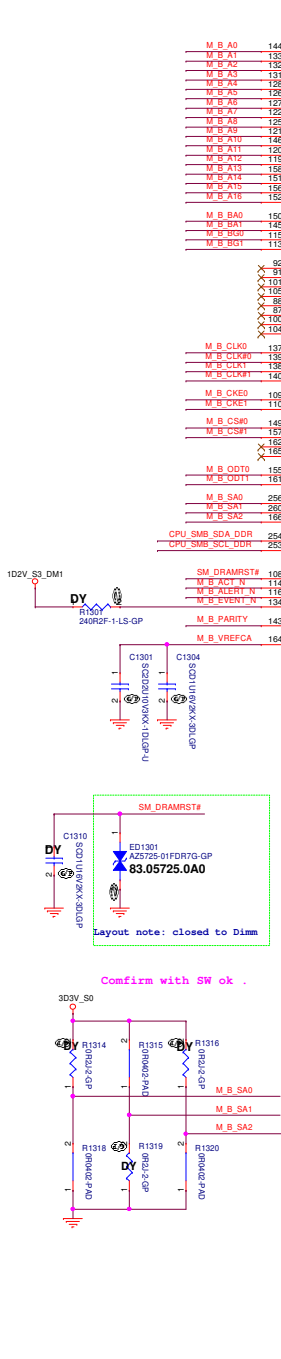
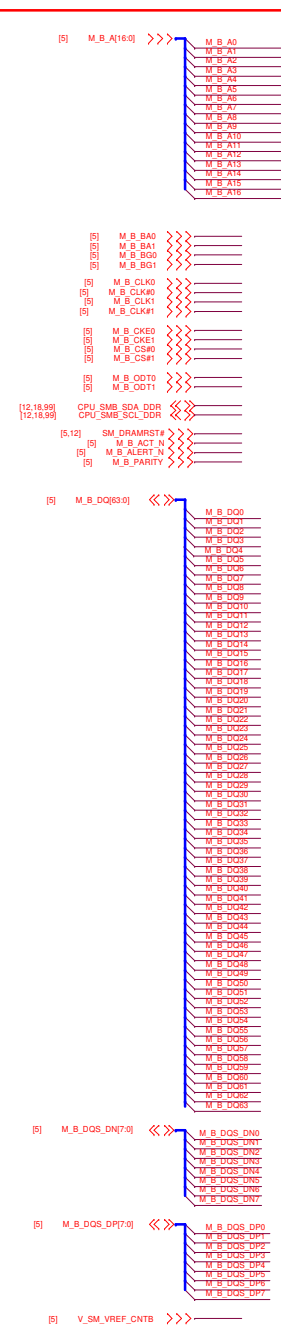
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File: **DDR (DDR4-CHA)**

Size: **Bandon / NorthBay 13"**

Date: Friday, February 15, 2019 Sheet 12 of 100

Main Func = Memory



WHL-U DDR4 SODIMM Decoupling

This recommendation assumes a 2CH, 1DPC (2 connector) implementation of SO-DIMMs.

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μF (size)
DDR4 SODIMM 1DPC	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 10 μF (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1 μF (0402)
		Place on VTT plane close to SODIMM	3x 330 μF (7343)
		Place on VTT plane close to SODIMM	2x 10 μF (0603)
	VTT	1 cap stuffed, 1 placeholder	4x 1 μF (0402)
	VPP	DIMM pin side, 1 per DIMM	2x 10 μF (0603)
	VDDSPD	DIMM pin side, 1 per DIMM	2x 1 μF (0402)
		Place close to DIMM	2x 0.1 μF (0402)
		Place close to DIMM	2x 2.2 μF (0402)

•Core Design•

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File: **DDR (DDR4-CHB)**

Size: **Document Number**

Date: **Friday, February 15, 2019**

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Rev: **X00**

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Title **(Reserved)_SODIMM _SODIMM4**

Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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Main Func = PCH

[19.27] SPKR <<<-
[20] NR_B BIT <<<-
[18.68.99] SPI_SL_CPU <<<-
[18.68.99] SPI_WP_CPU <<<-
[18.68] SPI_HOLD_CPU <<<-
[18] GPP_C2 <<<-
[6.99] CFG3 <<>>
[6.99] CFG4 <<>>
[15.21] GPD_7 <<<-

[20] GPP_D12 >>>-
[18] GPP_B23 >>>-
[15.21] GPD_7 >>>-
[21] GPP_H21 >>>-
[21] GPP_H23 >>>-
[6.99] ITP_PMODE >>>-
[19] HDA_SDO >>>-
[18] GPP_C5 >>>-
[20] GPP_B22 >>>-
[20.61] CNV_RGL_DT >>>-

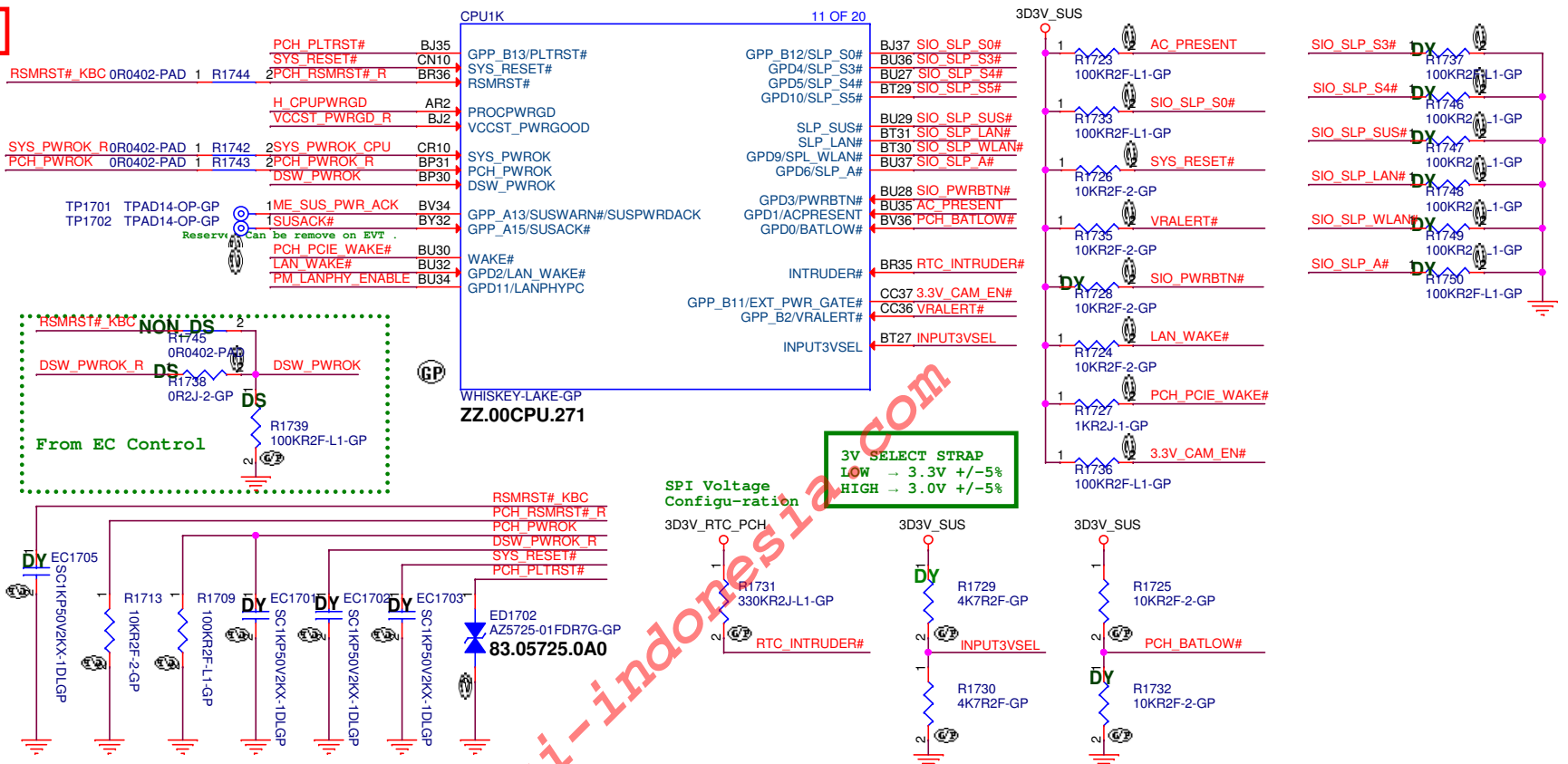
Description	Top Swap Override	No Reboot	TLS Confidentiality	BOOT BIOS STRAP (BBS)	ESPI OR LPC	BOOT HALT
GPIO	GPP_B14 / SFER / TIME_SYNC1 / GSP10_CS#	GPP_B18	GPP_C2	GPP_B22	GPP_C5	SPI0_MOSI
LOW	Disable (Default)	Disable (Default)	Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)	SPI SELECTED. (DEFAULT)	LPC SELECTED	
HIGH	Enable	Enable	Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.	LPC SELECTED FOR SYSTEM FLASH	HIGH: ESPI IS SELECTED FOR EC	This strap should sample HIGH.
	20 K \pm 30% internal pull-down.	20 K \pm 30% internal pull-down.	20 K \pm 30% internal pull-down.	20 K \pm 30% internal pull-down.	20 K \pm 30% internal pull-down.	20 K \pm 30% internal pull-up.

Description	JTAG ODT DISABLE	EXI BOOT STALL BYPASS	CONSENT STRAP	A0 PERSONALITY STRAP	Flash Descriptor Security Override	DFXTESTMODE
GPIO	GPP_D12	GPP_B23	SPI0_IO2	SPI0_IO3	HDA_SDO/12S0_TXD	ITP_PMODE
LOW	JTAG ODT DISABLED	ENABLED (BSSB 2+2)	ENABLED	ENABLED	Enable security measures, and security is not overridden	DFXTESTMODE DISABLE (DEFAULT)
HIGH	JTAG ODT ENABLED	DISABLED (BSSB 4 WIRE)	DISABLED	DISABLED	Disable security measures, and security is overridden	DFXTESTMODE ENABLE
	20 K \pm 30% internal pull-up	20 K \pm 30% internal pull-up	20 K \pm 30% internal pull-up	20 K \pm 30% internal pull-up	20 K \pm 30% internal pull-down.	20 K \pm 30% internal pull-up

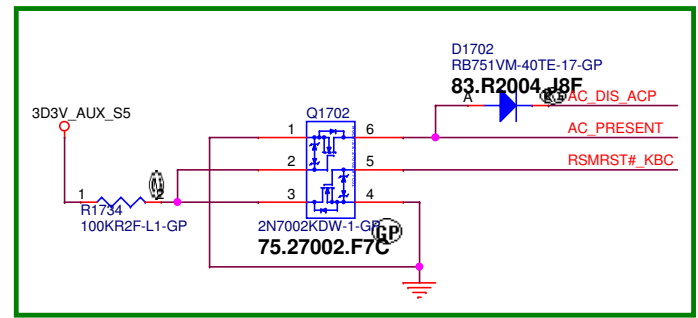
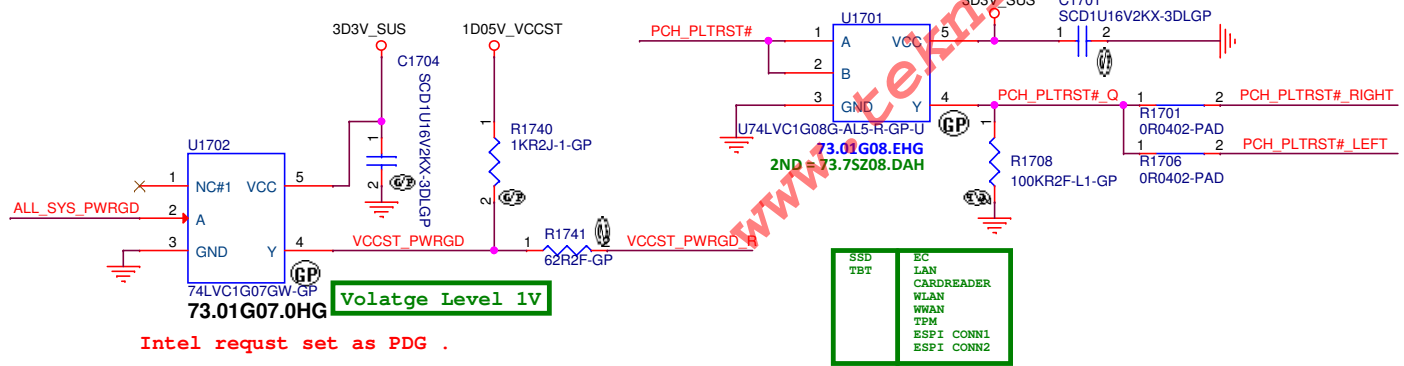
Description	RING OSCILLATOR BYPASS	XTAL FREQUENCY SELECT	M.2 CNVi Mode Select	MAF/SAF STRAP
GPIO	GPD7	GPP_H21	GPP_F4 / CNV_RGL_DT	GPP_H23
LOW	XTAL INPUT IS SINGLE ENDED	38.4/19.2MHZ (DEFAULT)	Integrated CNVi enabled	MAF ENABLE
HIGH	XTAL INPUT IS ATTACHED	24MHZ	Integrated CNVi disabled	SAF ENABLE

Main Func = PCH

[24,40,52,53,54]	SIO_SLP_SUS#	<<<<
[68]	SIO_SLP_S5#	<<<<
[40,51,68]	SIO_SLP_S4#	<<<<
[24,40,51,68,71]	SIO_SLP_S3#	<<<<
[68]	SIO_SLP_A#	<<<<
[40,54,68,91]	SIO_SLP_S0#	<<<<
[40]	SIO_SLP_WLAN#	<<<<
[40]	SIO_SLP_LAN#	<<<<
[68,99]	SYS_RESET#	<<<<
[24]	DSW_PWROK_R	<<<<
[46]	PCH_PWROK	<<<<
[24]	SYS_PWROK_R	<<<<
[24,99]	SIO_PWRBTN#	>>>>
[24]	AC_PRESENT	<<<<
[24,97]	LAN_WAKE#	<<<<
[24,62,71]	PCH_PCIE_WAKE#	<<<<
[97]	PM_LANPHY_ENABLE	<<<<
[18,24]	RTCRST_ON	>>>>
[24,64,99]	RSMRST#_KBC	>>>>
[24]	ALL_SYS_PWRGD	>>>>
[33,61,62,91,97]	PCH_PLTRST#_RIGHT	<<<<
[63,71,99]	PCH_PLTRST#_LEFT	<<<<
[21,24,40,54,91]	CPU_C10_GATE#	<<<<
[3]	H_CPUUPWRGD	<<<<
[40]	3.3V_CAM_EN#	>>>>
[44]	AC_DIS_ACP	>>>>



PCH_PWROK: pull-up resistance should be in range 1/10th of pull down resistance



<Core Design>

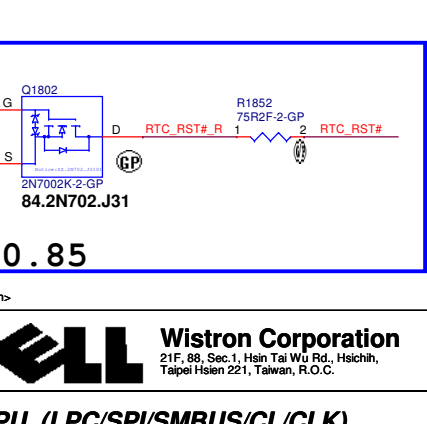
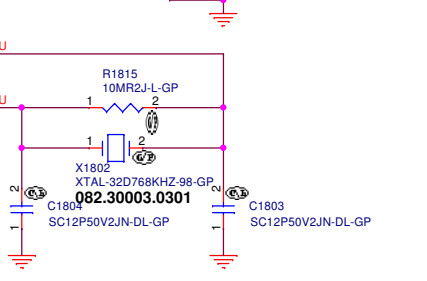
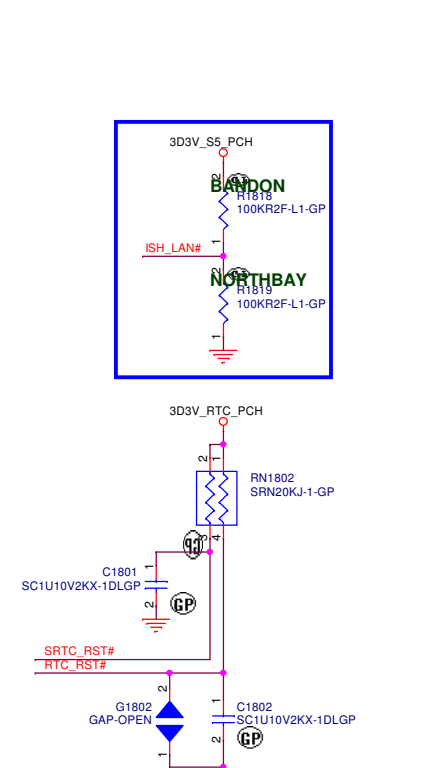
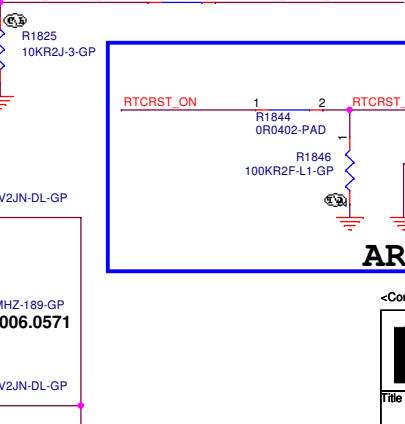
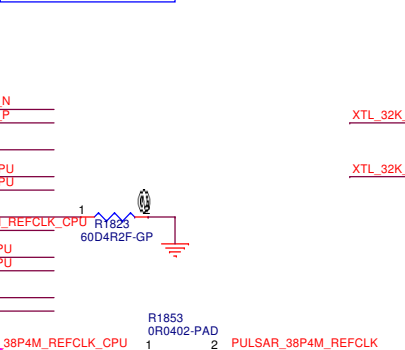
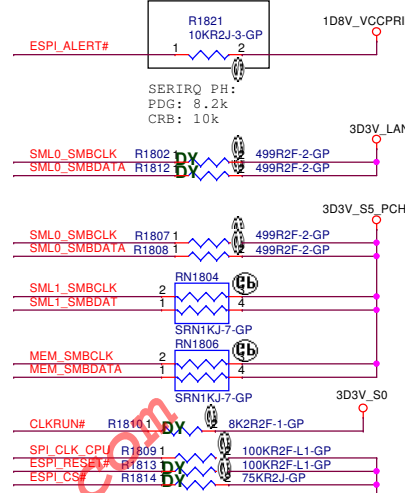
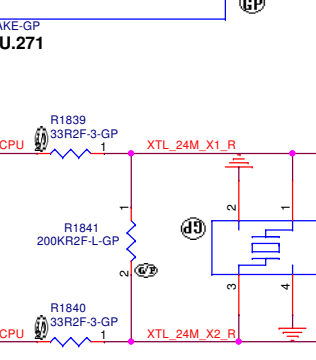
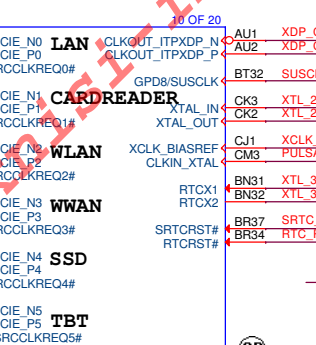
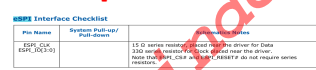
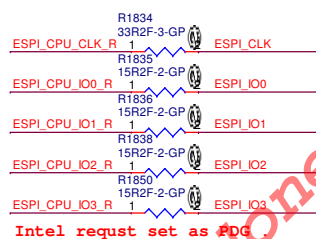
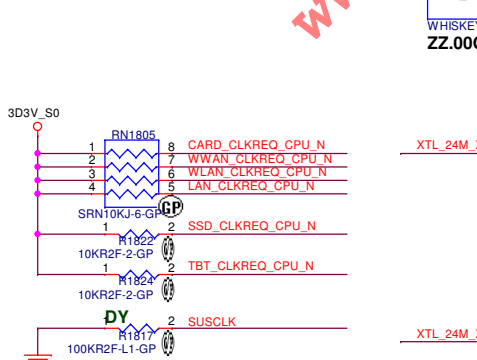
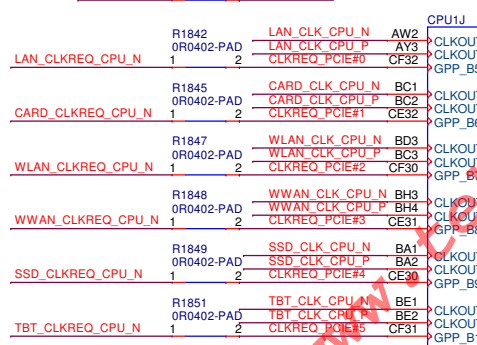
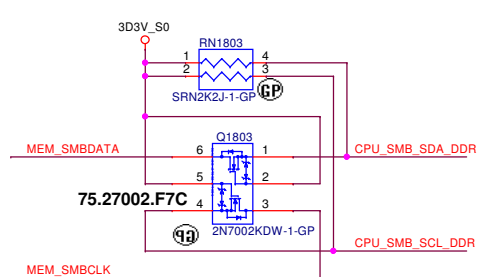
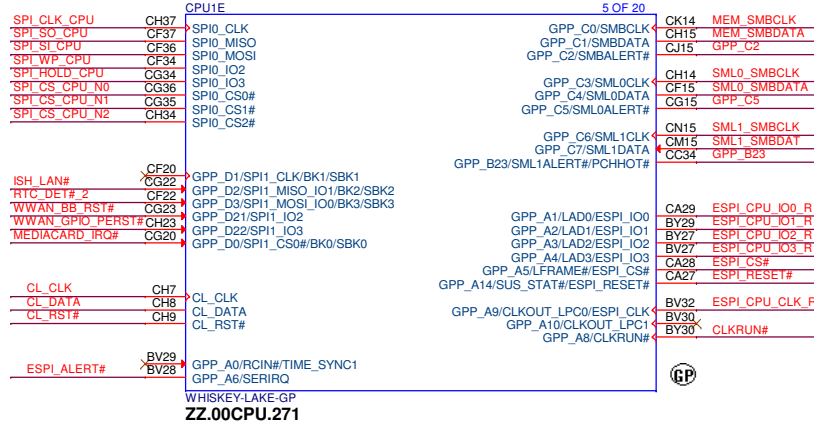
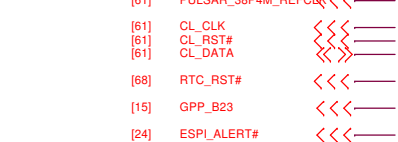
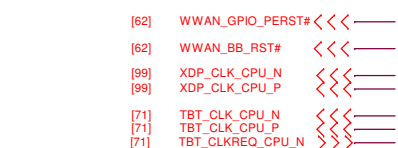
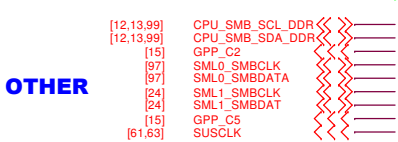
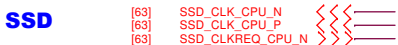
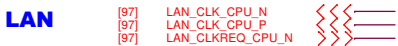
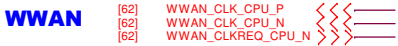
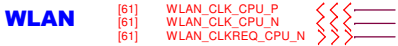
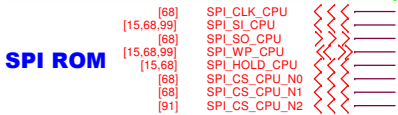
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Title **CPU_(POWER MANAGEMENT)**

Size Custom Document Number **Bandon / NorthBay 13"** Rev **X00**

Date: Friday, February 15, 2019 Sheet 17 of 106

Main Func = PCH



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CPU (LPC/SPI/SMBUS/CL/CLK)

Bandon / NorthBay 13"

Rev X00

Date: Friday, February 15, 2019

Sheet 18 of 106

Main Func = PCH

[27] HDA_SDIO <<< —
[27] HDA_SDOOUT_CODEC <<< —
[27] HDA_SYNC_CODEC <<< —
[27] HDA_BITCLK_CODEC <<< —
[15] HDA_SDO <<< —

[66] CONTACTLESS_DET# >>> —

[56] CAM_MIC_CBL_DET# >>> —

[29] SPK_DET# >>> —

[33] HOST_SD_WP# >>> —

[27] AUD_PWR_EN <<< —

[68] ME_FWP_PCH <<< —

[15,27] SPKR <<< —

[61] CLKREQ_CNV >>> —
[61] CNV_RF_RESET# >>> —

[65] KB_DET# <<< —

[62] WWAN_GPIO_WAKE# <<< —

[71] TBT_CIO_PLUG_EVENT# <<< —

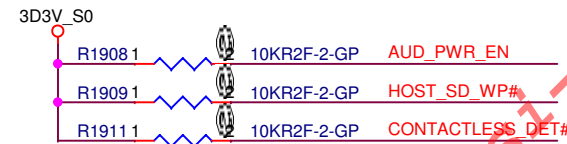
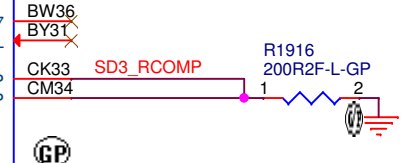
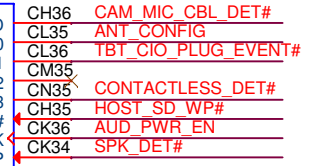
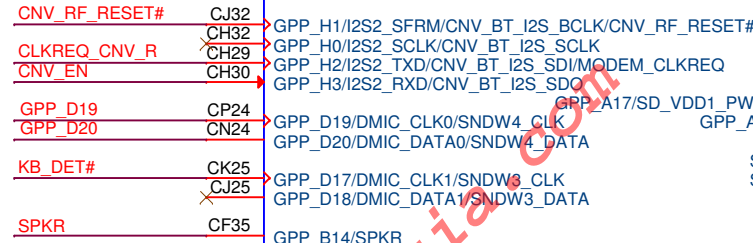
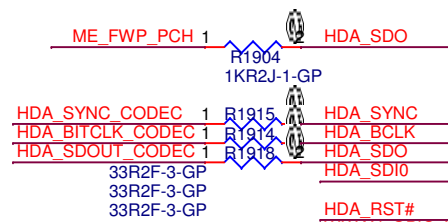
[56] DMIC_SDA_CODEC_CPU <<< —

[56] DMIC_SCL_CODEC_CPU <<< —

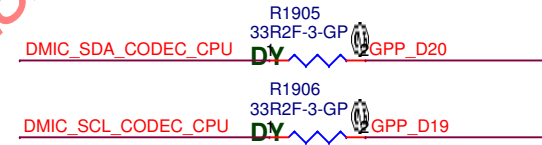
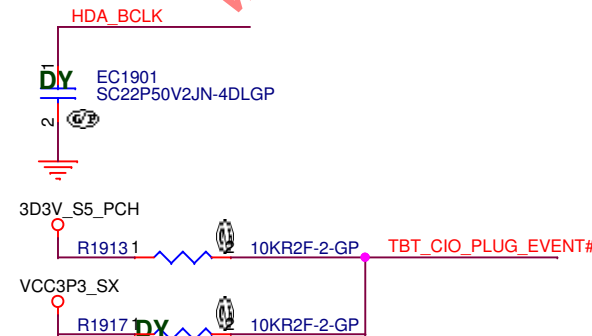
[62] ANT_CONFIG >>> —

[61] CNV_EN <<< —

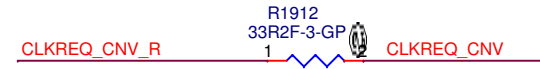
[27] HDA_RST# <<< —



GBT0.5 change to 1.8V



Reserve for Dmic connect to PCH



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (AUDIO/SDIO/SDXC)

Size
A4

Document Number

Bandon / NorthBay 13"

Rev
X00

Date: Friday, February 15, 2019

Sheet 19 of 106

Main Func = PCH

[68] CPU_UART2_TXD <<< <<<
[68] CPU_UART2_RXD <<< <<<
[55] CPU_I2C_SDA_TS <<< <<<
[55] CPU_I2C_SCL_TS <<< <<<
[65] CPU_I2C_SDA_TP <<< <<<
[65] CPU_I2C_SCL_TP <<< <<<

[69,70] CPU_I2C_SDA_SENSOR <<< <<<
[69,70] CPU_I2C_SCL_SENSOR <<< <<<

[62] CPU_I2C_SDA_GNSS <<< <<<
[62] CPU_I2C_SCL_GNSS <<< <<<

[69] GSEN_INT1 <<< <<<
[70] LNG2DMTR_INT1 <<< <<<

[24] NB_MODE# <<< <<<
[24] LID_CL#_NB_R >>> >>>
[24] LID_CL#_TAB_R >>> >>>

[24] LID_CL#_TAB_R >>> >>>
[15,20] NRB_BIT >>> >>>

[91] TPM_PIRQ# <<< <<<
[40] PCH_3.3V_TS_EN <<< <<<
[15] GPP_B22 <<< <<<
[55] TS_INT# <<< <<<

[24] SIO_EXT_WAKE# <<< <<<
[55] LCD_CBL_DET# >>> >>>

[61] CNV_BRI_RSP <<< <<<
[15,61] CNV_RGI_DT <<< <<<
[61] CNV_RGI_DT <<< <<<
[61] CNV_RGI_RSP <<< <<<

[15,20] NRB_BIT <<< <<<
[15] GPP_D12 <<< <<<

[56] IR_CAM_DET# >>> >>>
[62] WWAN_FULL_PWR_EN# <<< <<<

[54] PRIM_CORE_OPT_DIS <<< <<<
[18,25] RTC_DET# >>> >>>

[15,20] NRB_BIT <<< <<<
[15] GPP_D12 <<< <<<

[56] IR_CAM_DET# >>> >>>
[62] WWAN_FULL_PWR_EN# <<< <<<

[54] PRIM_CORE_OPT_DIS <<< <<<
[18,25] RTC_DET# >>> >>>

[56] IR_CAM_DET# >>> >>>
[62] WWAN_FULL_PWR_EN# <<< <<<

[54] PRIM_CORE_OPT_DIS <<< <<<
[18,25] RTC_DET# >>> >>>

[56] IR_CAM_DET# >>> >>>
[62] WWAN_FULL_PWR_EN# <<< <<<

[54] PRIM_CORE_OPT_DIS <<< <<<
[18,25] RTC_DET# >>> >>>

[56] IR_CAM_DET# >>> >>>
[62] WWAN_FULL_PWR_EN# <<< <<<

[54] PRIM_CORE_OPT_DIS <<< <<<
[18,25] RTC_DET# >>> >>>

[56] IR_CAM_DET# >>> >>>
[62] WWAN_FULL_PWR_EN# <<< <<<

[54] PRIM_CORE_OPT_DIS <<< <<<
[18,25] RTC_DET# >>> >>>

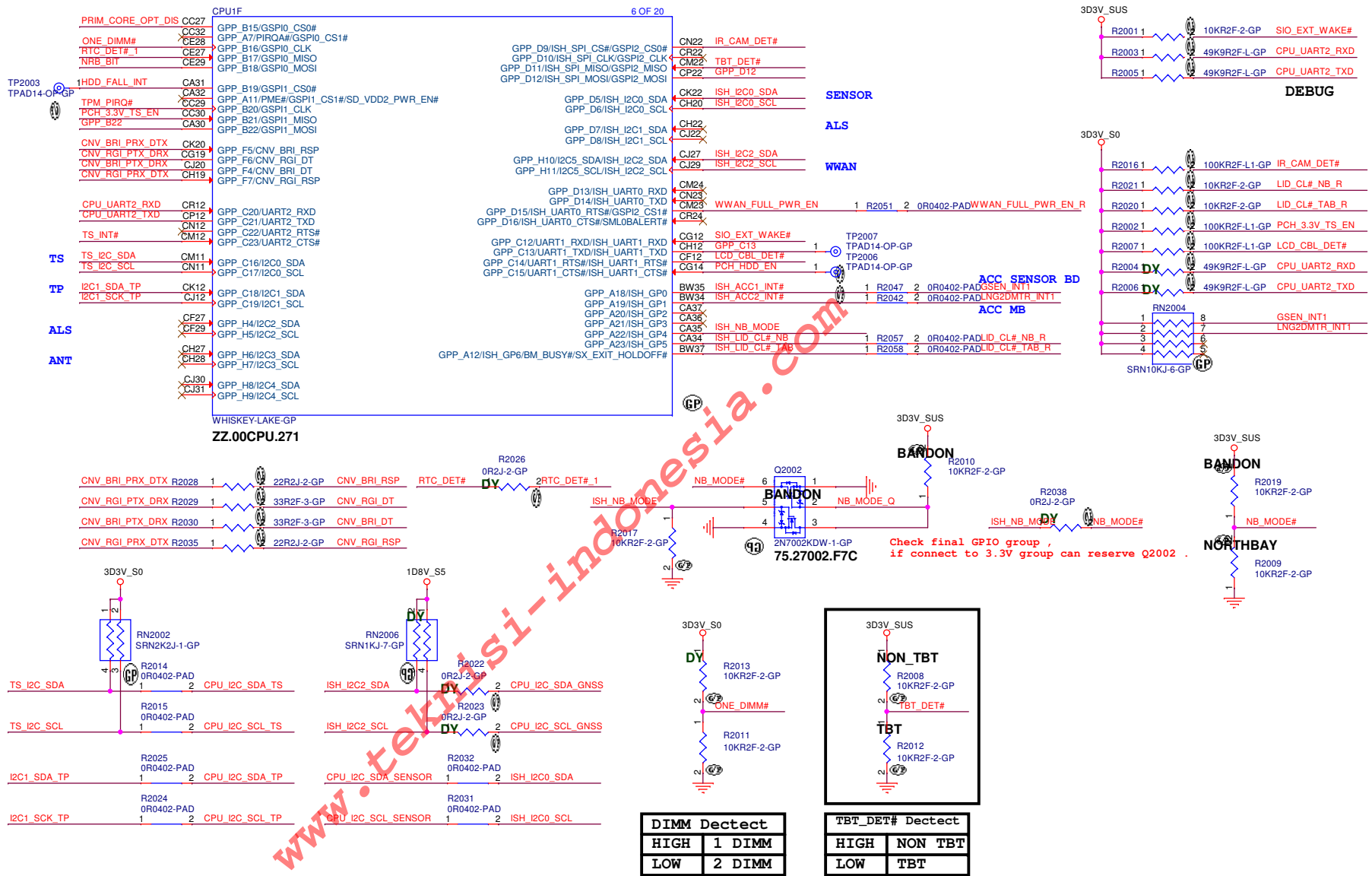
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[18,25] RTC_DET# >>> >>>

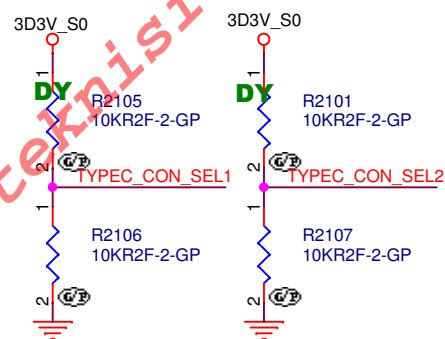
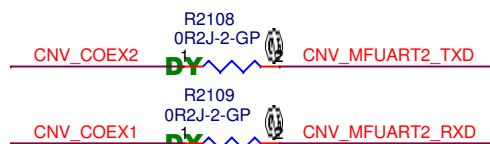
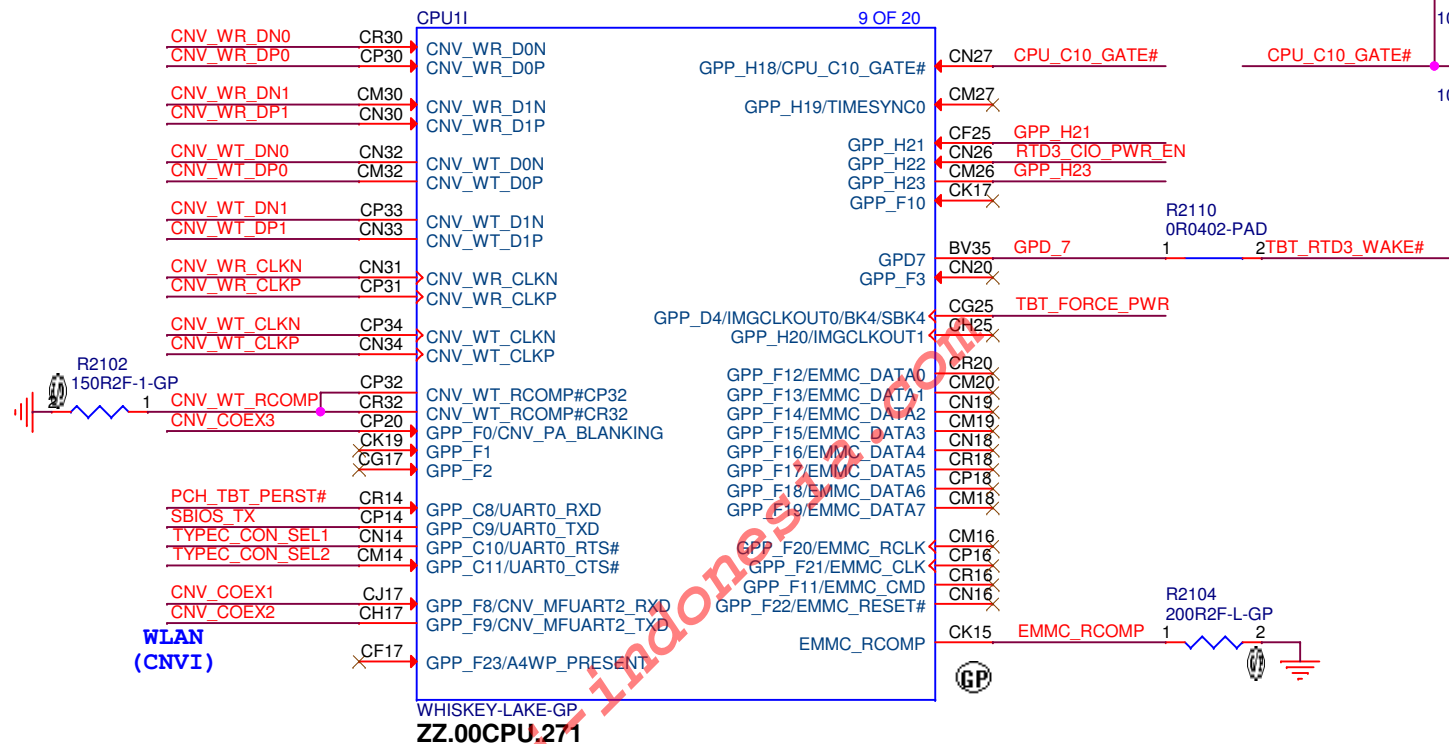
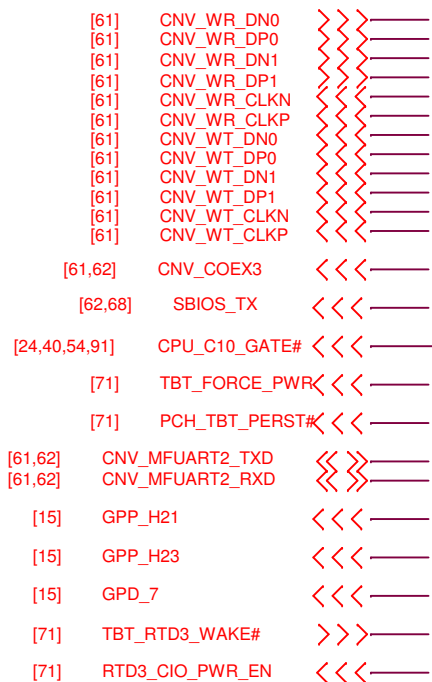
[56] IR_CAM_DET# >>> >>>
[62] WWAN_FULL_PWR_EN# <<< <<<

[54] PRIM_CORE_OPT_DIS <<< <<<
[18,25] RTC_DET# >>> >>>

[56] IR_CAM_DET# >>> >>>
[62] WWAN_FULL_PWR_EN# <<< <<<



Main Func = PCH



Vendor	JAE	FOXCON	TBD	TBD
TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH

<Core Design>



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Title

CPU (POWER1)

Size
A4

Document Number

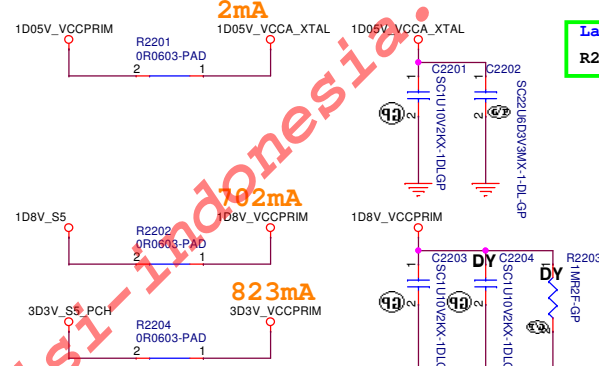
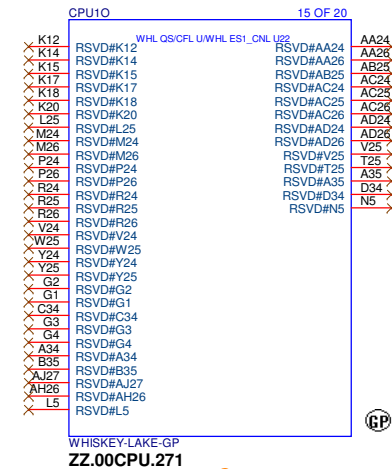
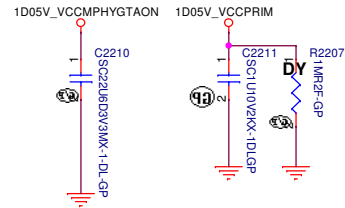
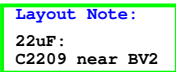
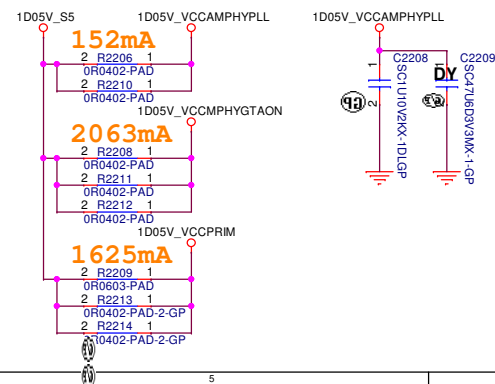
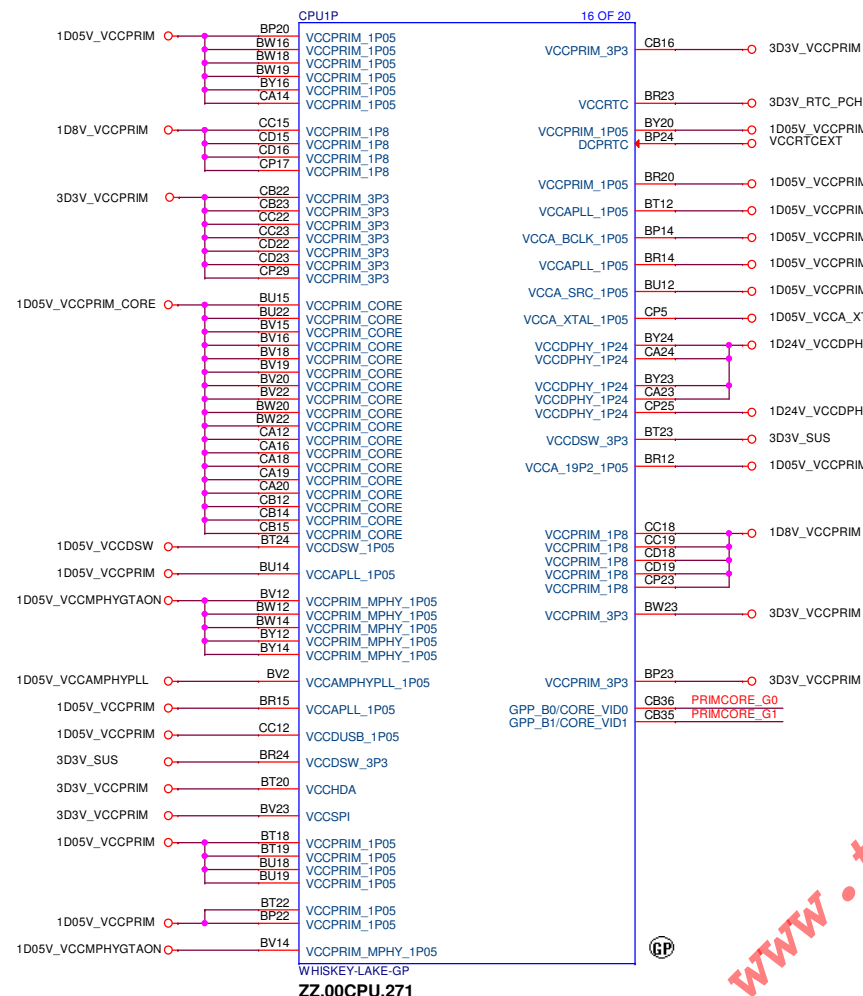
Bandon / NorthBay 13"

Rev
X00

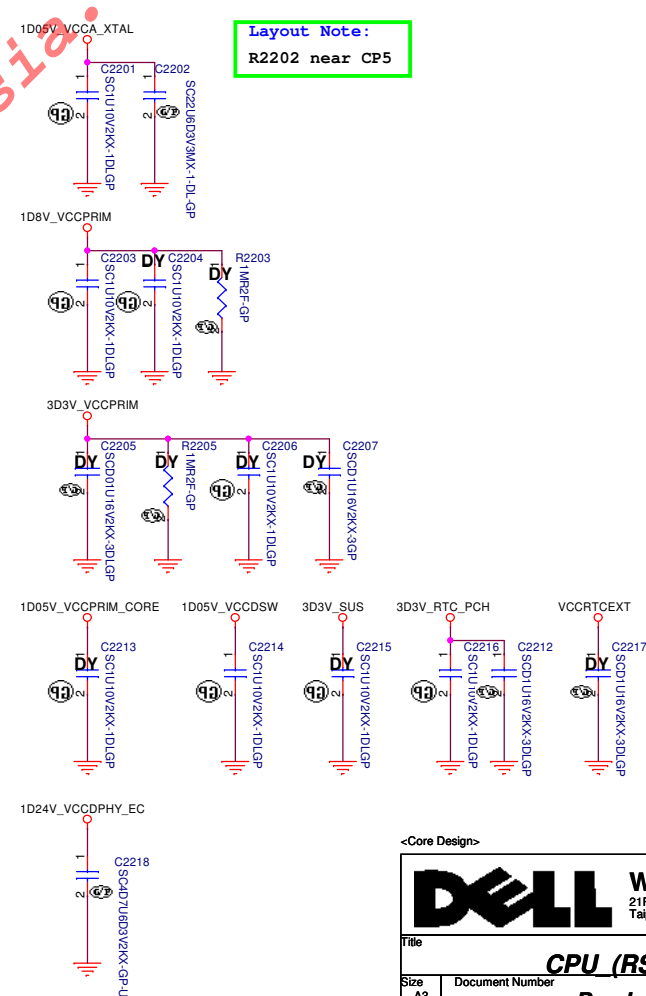
Date: Friday, February 15, 2019

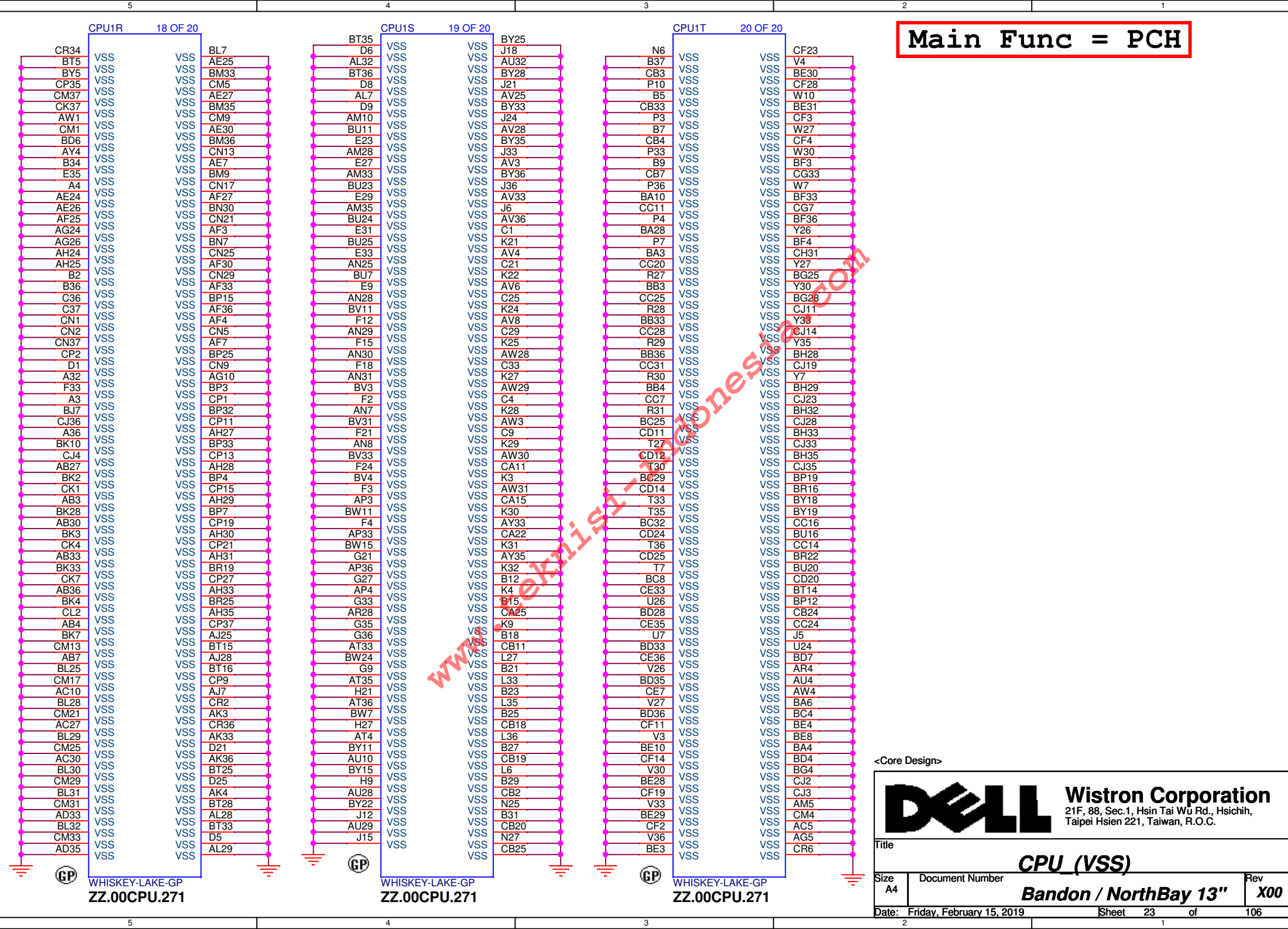
Sheet 21 of 106

```
[54] PRIMCORE_G0    >>>_____
[54] PRIMCORE_G1    >>>_____
```

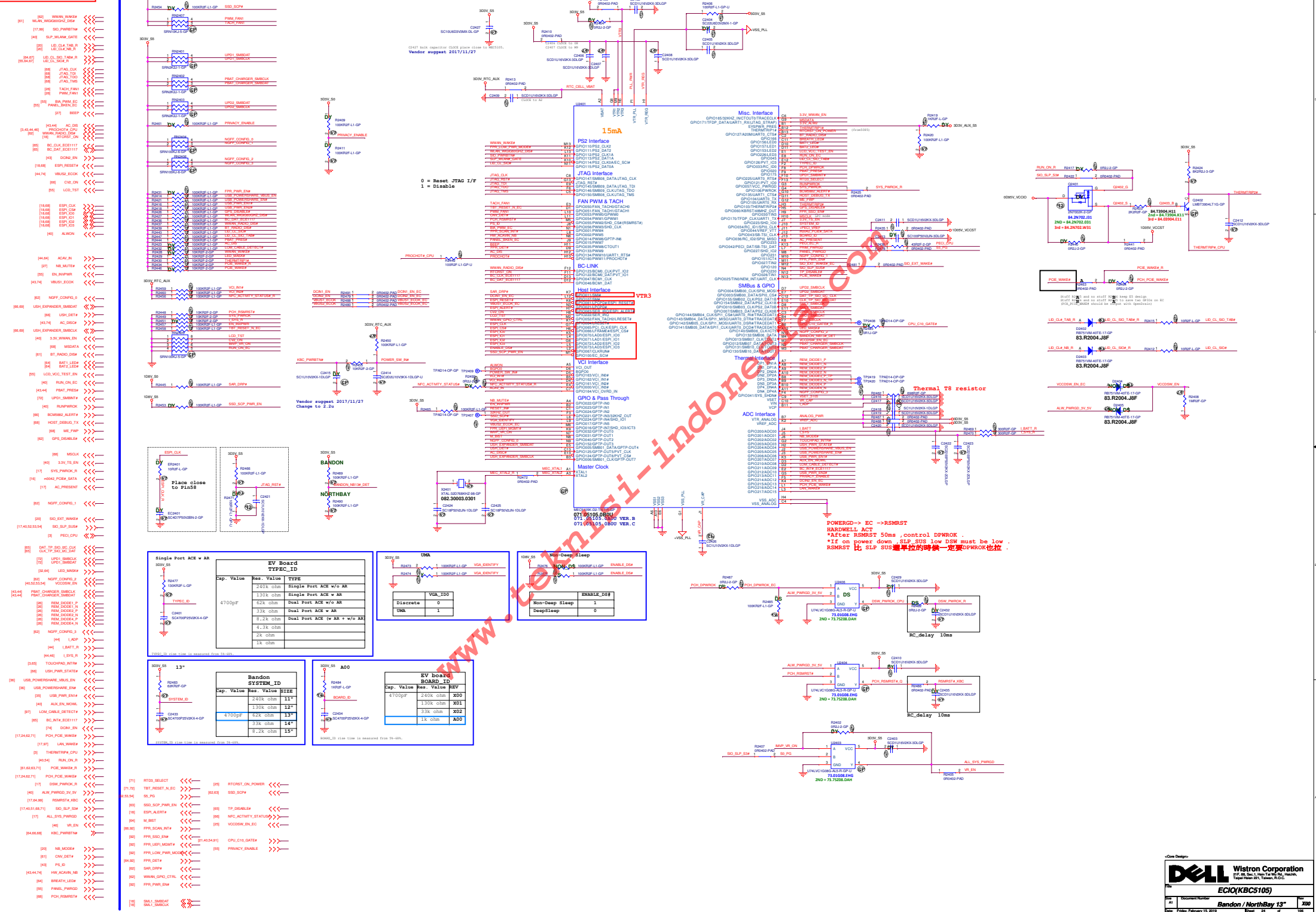


Layout Note:
R2202 near CP5

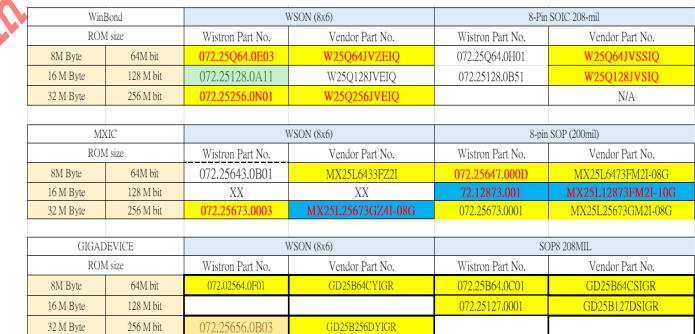




Main Func = EC



SYSTEM SPI ROM



X09 design DS3 Non-DS3 with RTC power gating



Flash/RTC

Rev

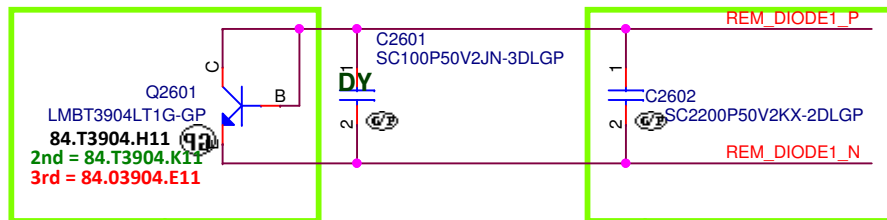
Bandon / NorthBay 13"

106

Main Func = Thermal / FAN

[24] REM_DIODE1_P
[24] REM_DIODE1_N
[24] REM_DIODE2_P
[24] REM_DIODE2_N

[24] REM_DIODE4_P
[24] REM_DIODE4_N
[24] PWM_FAN1
[24] TACH_FAN1

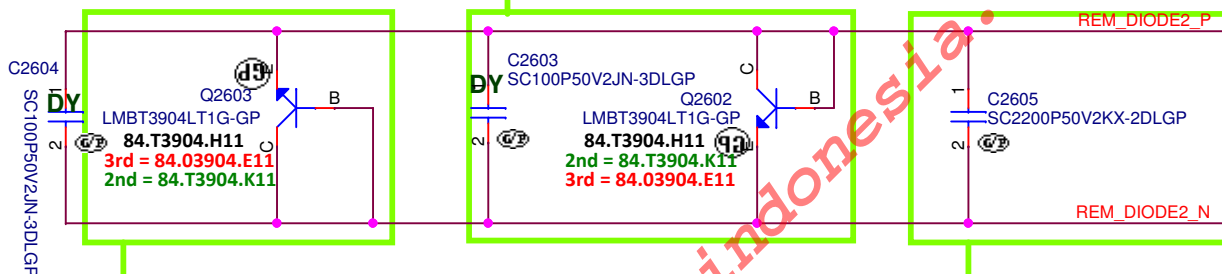


Layout Note: Place to CPU

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC

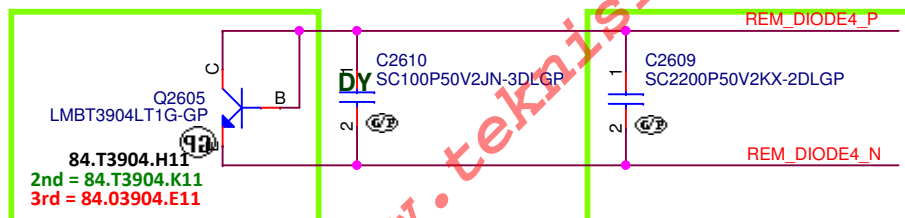
Layout Note: Close to WWAN/2nd SSD



Layout Note: Place to DIMM

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

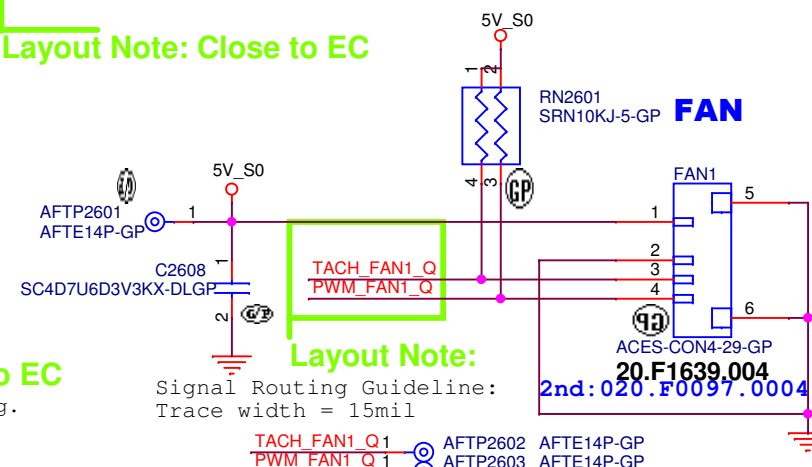
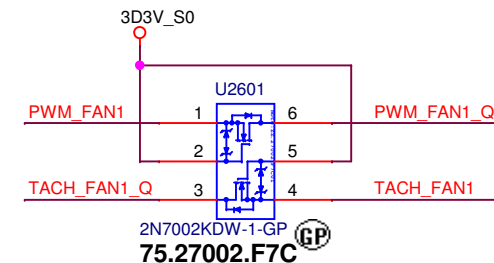
Layout Note: Close to EC



Layout Note: Place to V.R

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC



Signal Routing Guideline:
Trace width = 15mil

TACH_FAN1_Q 1
PWM_FAN1_Q 1

<Core Design>



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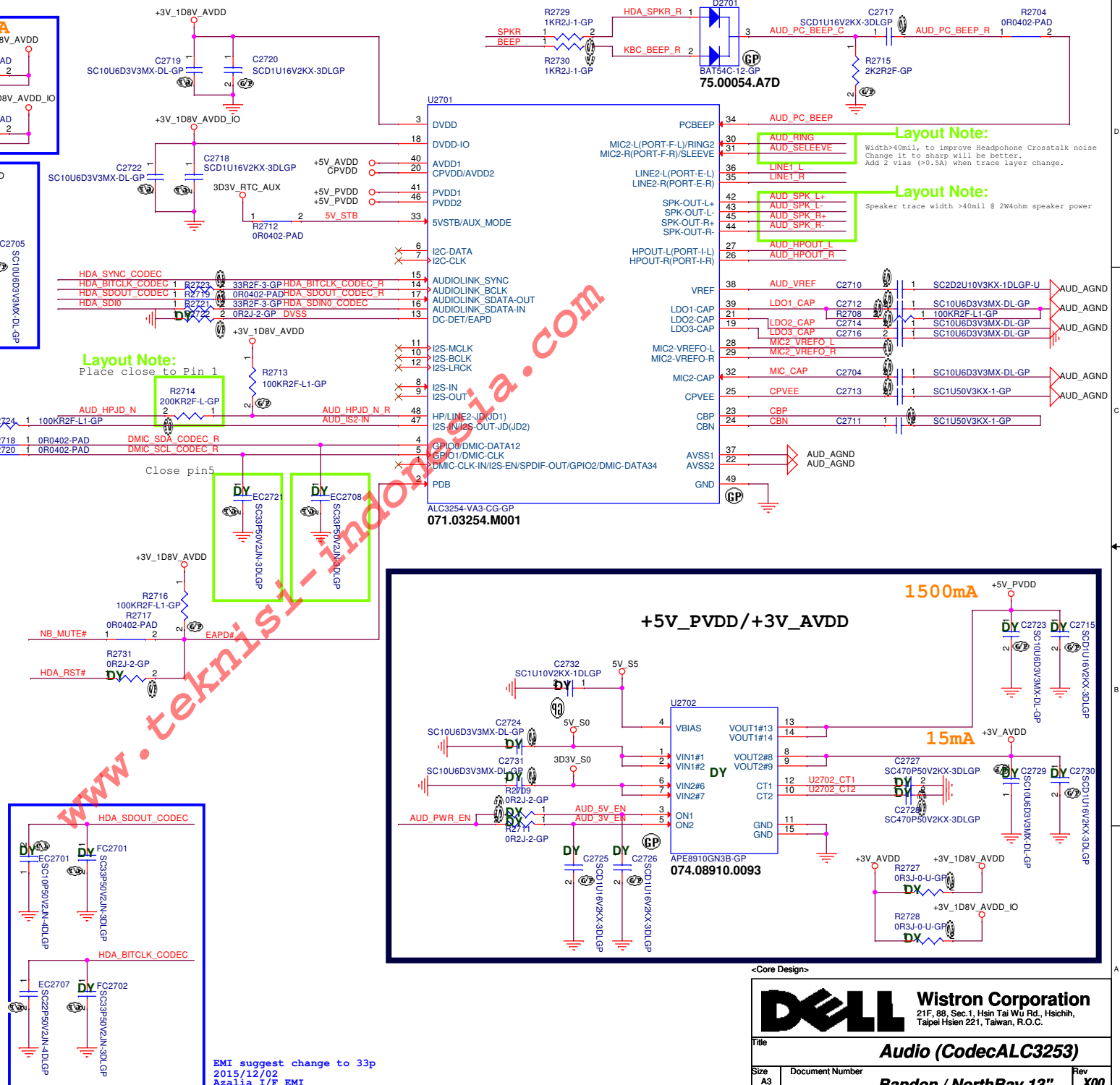
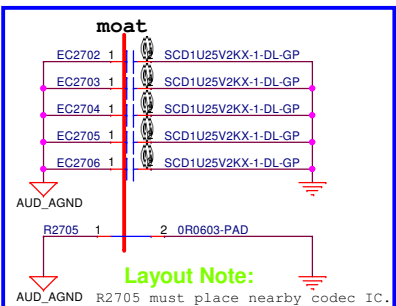
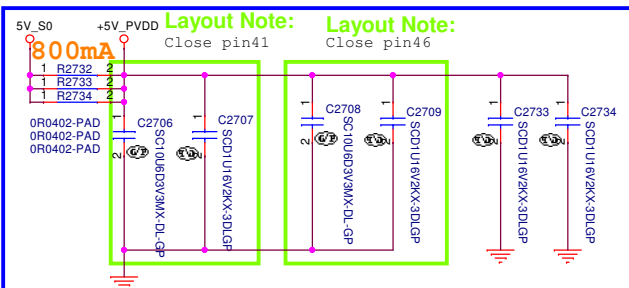
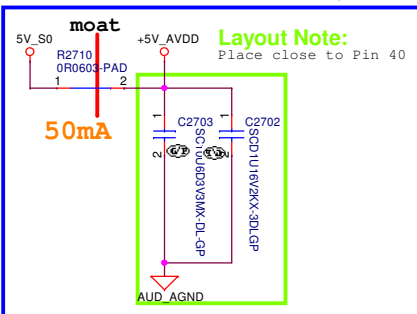
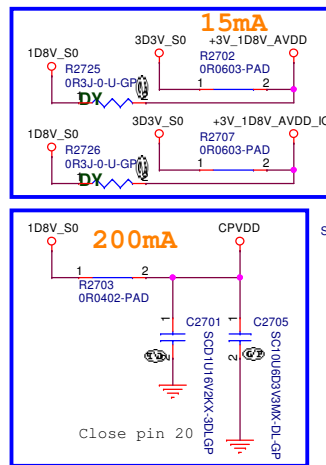
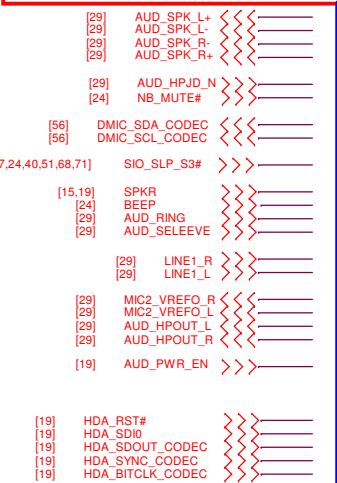
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title INT IO (Thermal/Fan)

Size A4 Document Number Bandon / NorthBay 13" Rev X00


Date: Friday, February 15, 2019 Sheet 26 of 106

Main Func = Audio



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Title

Audio (RSVD) (Audio AMP)

Size
A4

Document Number

Date: Friday, February 15, 2019


Rev
X00

Bandon / NorthBay 13"

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio (RSVD)			
Size A4	Document Number Bandon / NorthBay 13"		Rev X00
Date: Friday, February 15, 2019		Sheet 30 of	106

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title LAN (RSVD) (Giga_RTL8151GD)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
Date: Friday, February 15, 2019		Sheet 31 of 106

Main Func = LAN

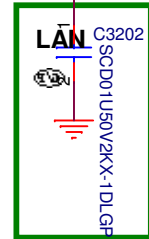
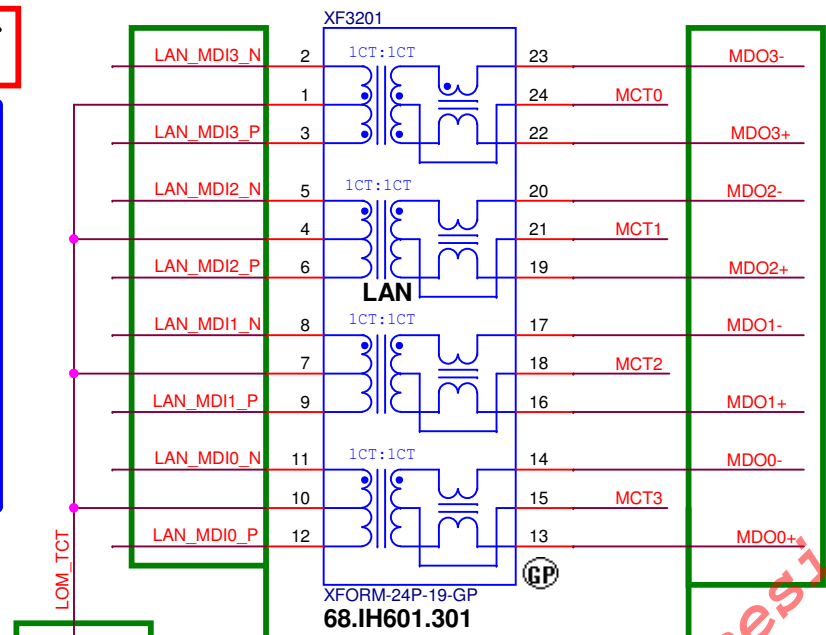
[24,64] LED_MASK#
 [97] LAN_0_GREEN_LINK_N
 [97] LAN_1_AMBER_ACT_N

[97] LAN_MDI0_P
 [97] LAN_MDI0_N

[97] LAN_MDI1_P
 [97] LAN_MDI1_N

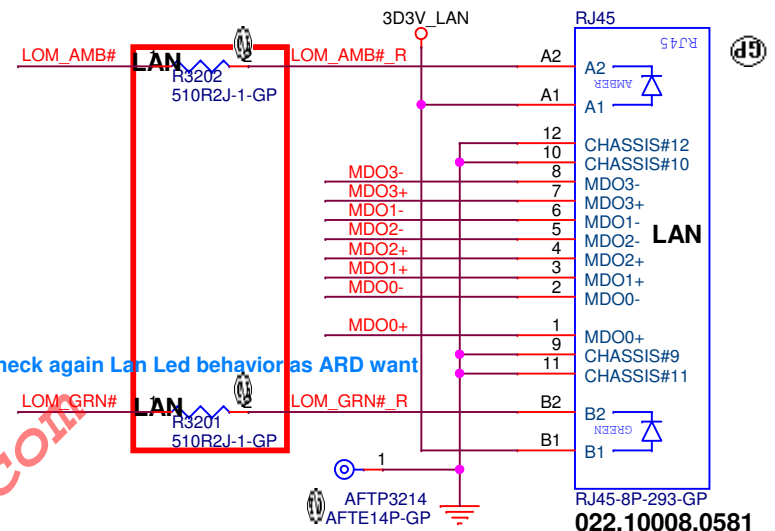
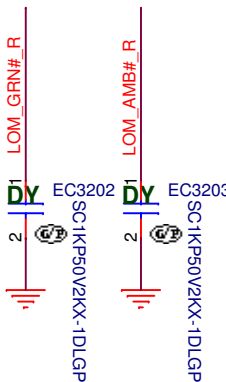
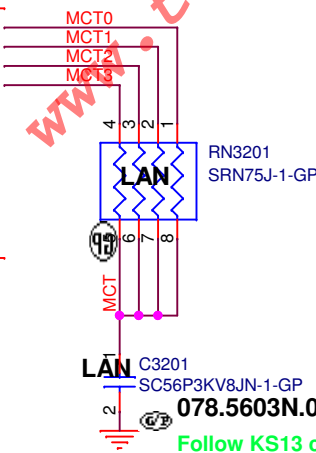
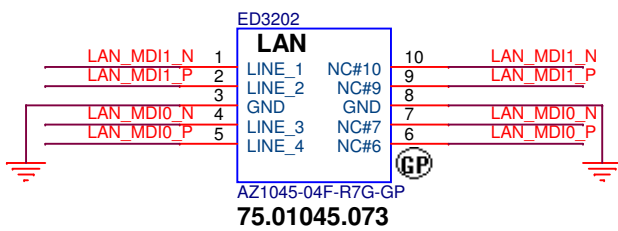
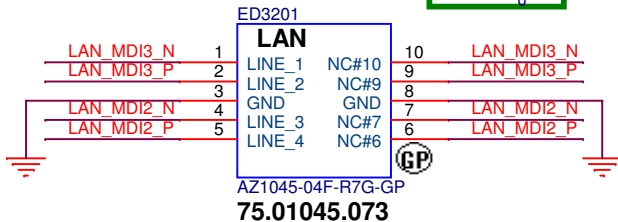
[97] LAN_MDI2_P
 [97] LAN_MDI2_N

[97] LAN_MDI3_P
 [97] LAN_MDI3_N

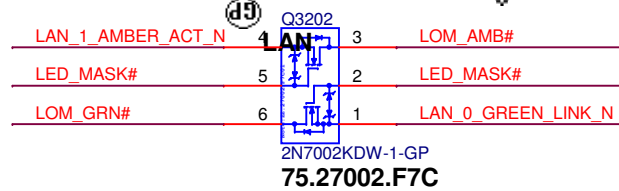
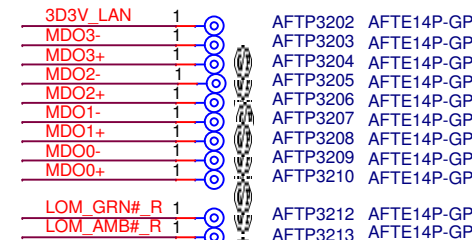


Layout note:
 30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF



Check again Lan Led behavior as ARD want



- LED0 (010): Green = Indicates Link connection established (located on left-hand side of connector)
- LED1 (011): Amber = Blinking when network activity (located on right-hand side of connector)

<Core Design>

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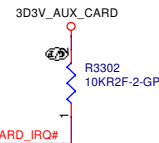
Title **LAN (RJ45+Transformer)**

Size A4 Document Number **Bandon / NorthBay 13"** Rev **X00**

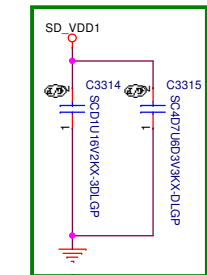
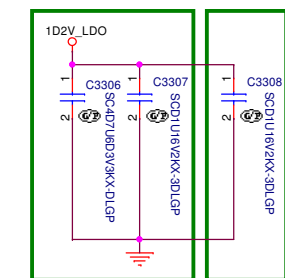
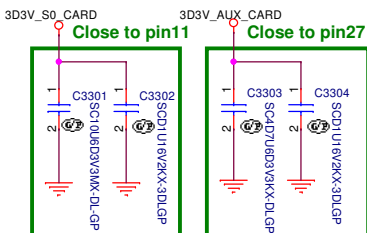
Date: Friday, February 15, 2019 Sheet 32 of 106

3D3V_S0_CARD

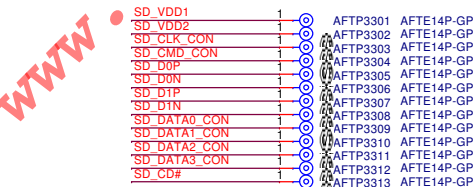
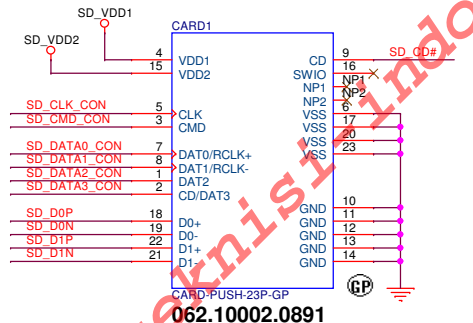
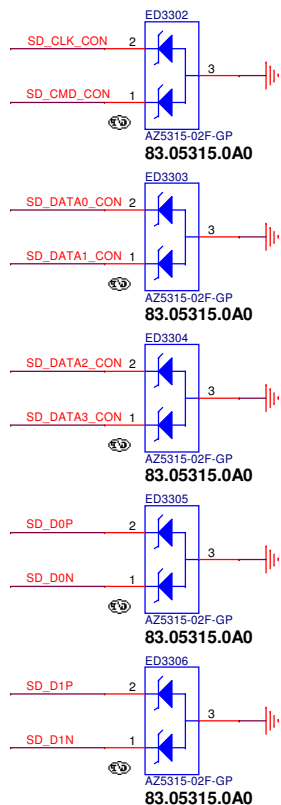
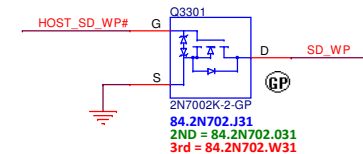
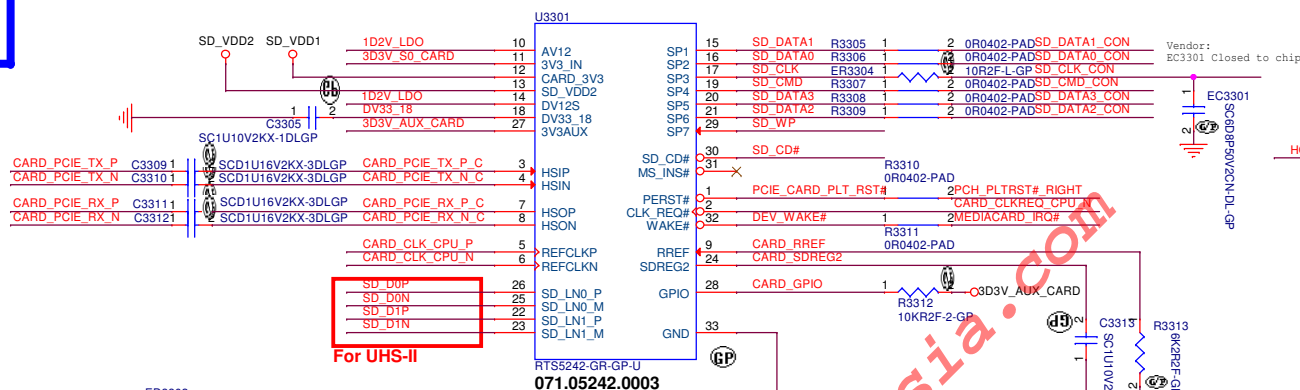
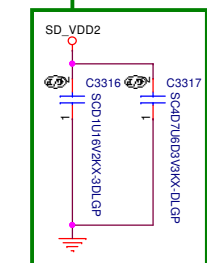
850mA



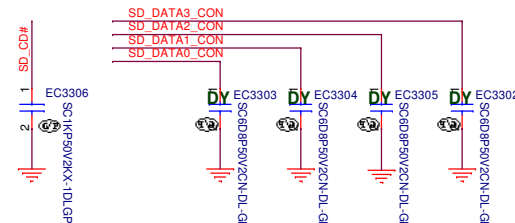
3D3V_S0_CARD 3D3V_AUX_CARD
Close to pin11 Close to pin27



Layout Note:Close to Card Reader CONN



以上測點不可拉分支型式



DELL


Title	CARDREADER (SDIO/SD Conn)
-------	----------------------------------

Size A3	Document Number Bender / North Bay 12"	Rev Y00
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Date: Friday, February 15, 2019 Sheet 33 of 106

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<Core Design>

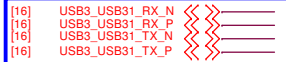
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title USB (RSVD) (USB2.0 CONN)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
Date: Friday, February 15, 2019		Sheet 34 of 106

Main Func = USB 3.0

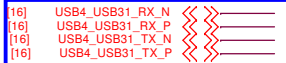
USB4/USB30-3/USB20-3/PowerShare

EXT Port1 Right Side, Support Power Share

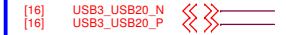
USB3.1 PORT1



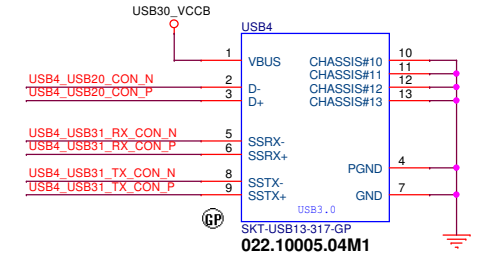
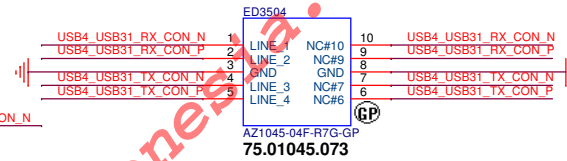
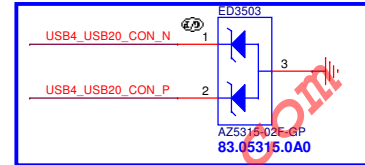
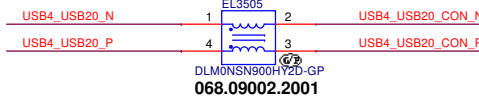
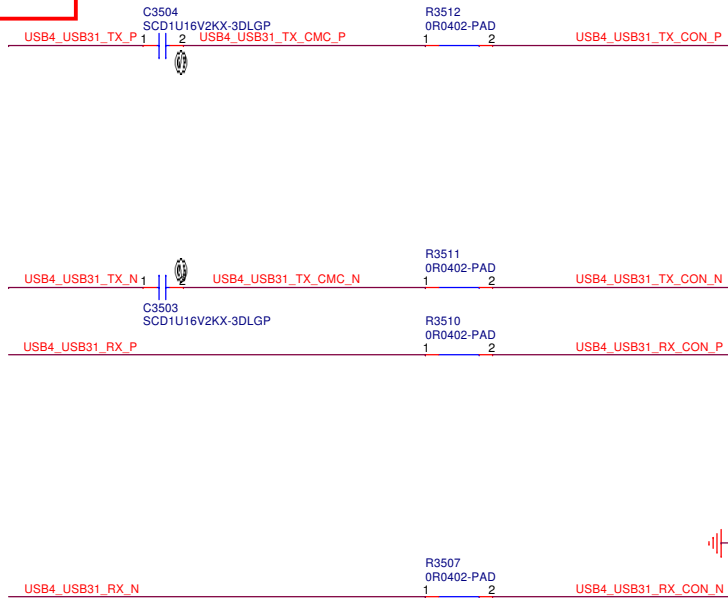
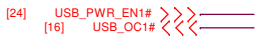
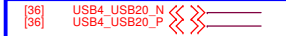
USB3.1 PORT2



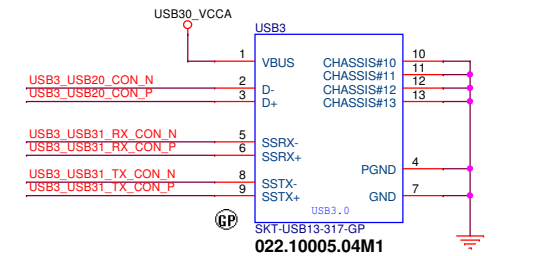
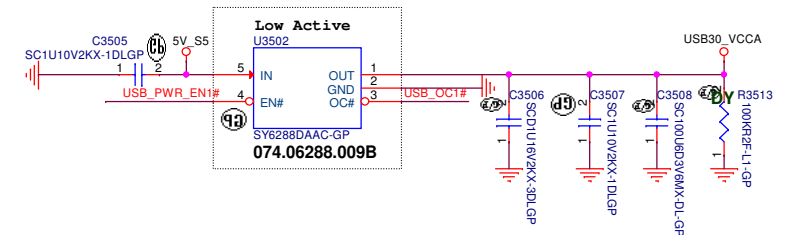
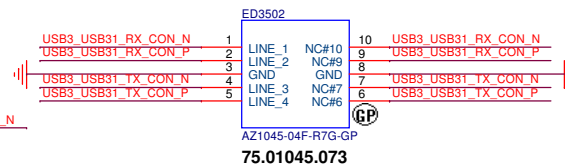
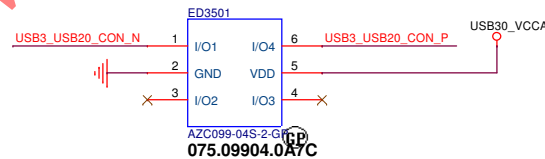
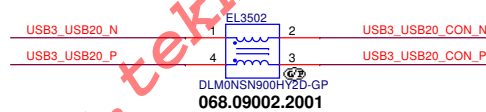
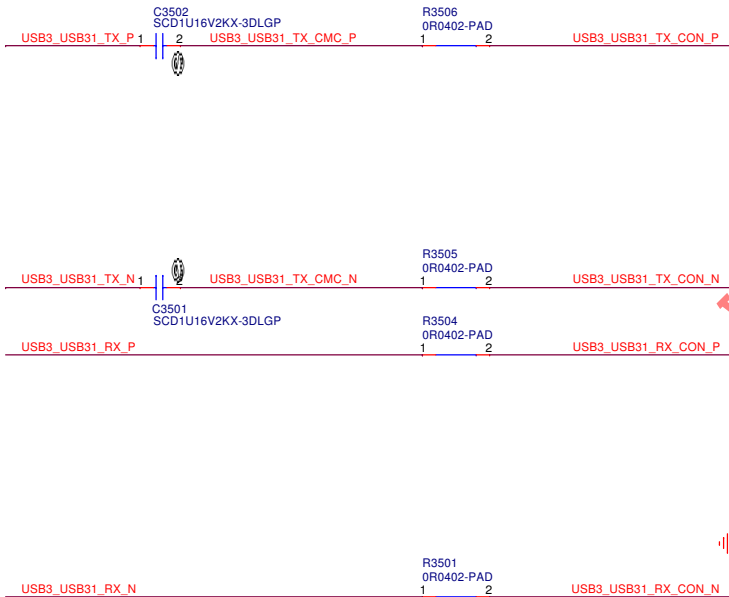
USB2.0 port2



USB2.0 port1




USB3/USB30-3/USB20-2




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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title USB (RSVD) (PCIE to USB3.0)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
Date: Friday, February 15, 2019		Sheet 37 of 106

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title USB (RSVD)(USB3.0 Redriver)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
Date: Friday, February 15, 2019		Sheet 38 of 106

Main Func =

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<Core Design>



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Title

Sequence (RSVD)

Size
A4

Document Number

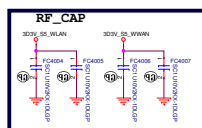
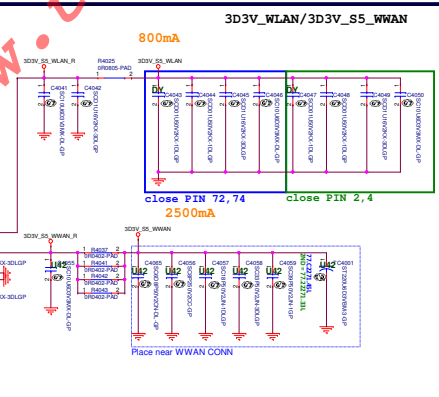
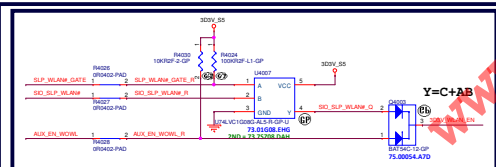
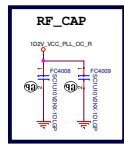
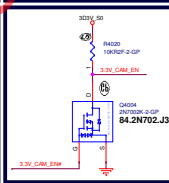
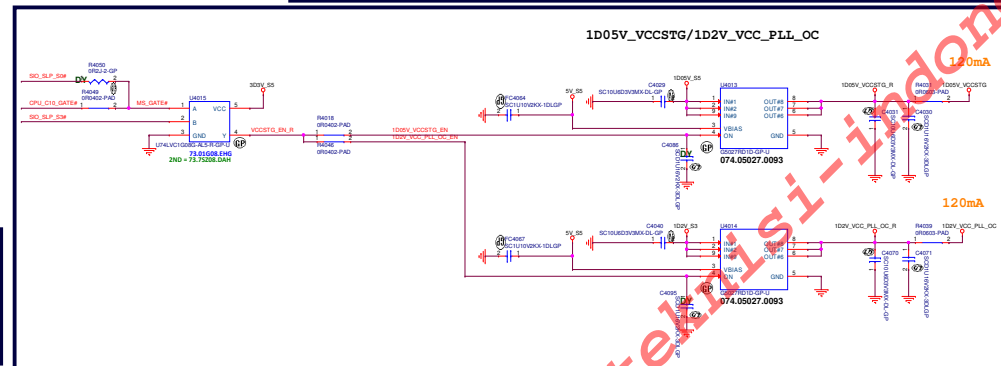
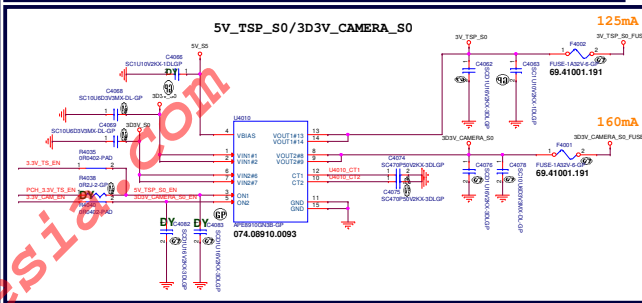
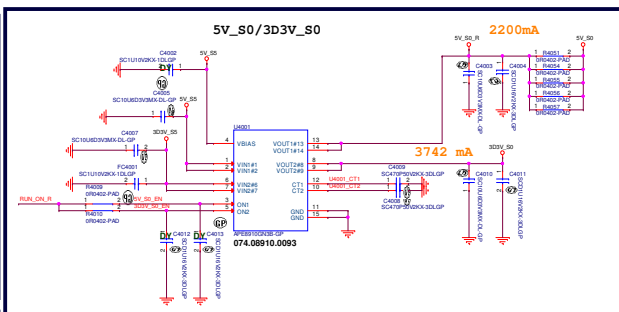
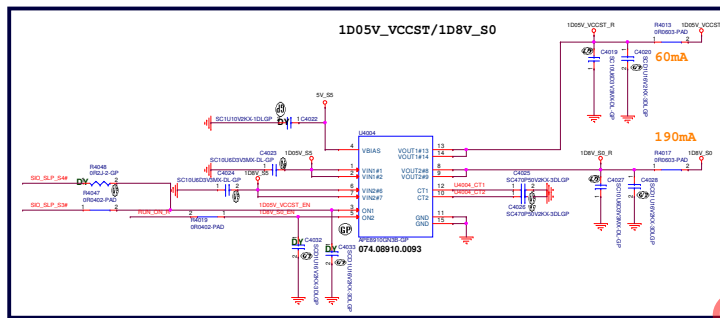
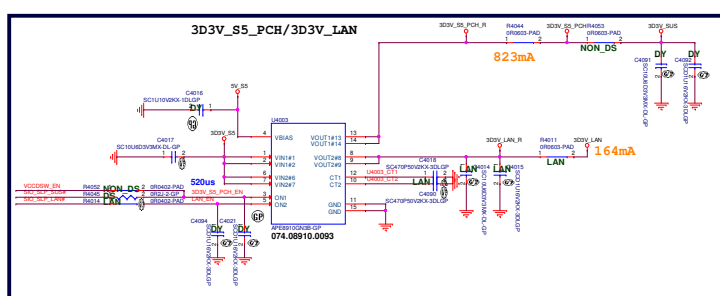
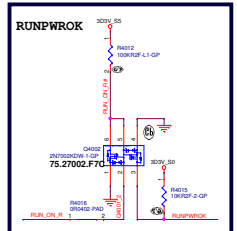
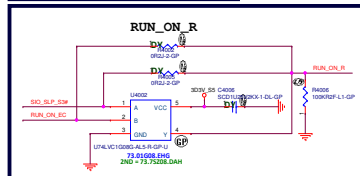
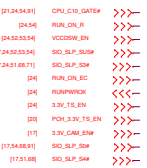
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[24]	ALWON	>>>—
[45]	3V5V_EN	<<<—
[45]	303V_PG	>>>—
[45]	5V_PG	>>>—
	ALW_PWRIGD_3V_5V	<<<—
[17]	SIO_SLP_LAN#	>>>—
[24]	SLP_WLAN#_GATE	>>>—
[17]	SIO_SLP_WLAN#	>>>—
	AUX_EN_WOWL	>>>—
[24]	3.5V_WWAN_EN	>>>—




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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Sequence (RSVD) (DS3/S0ix)		
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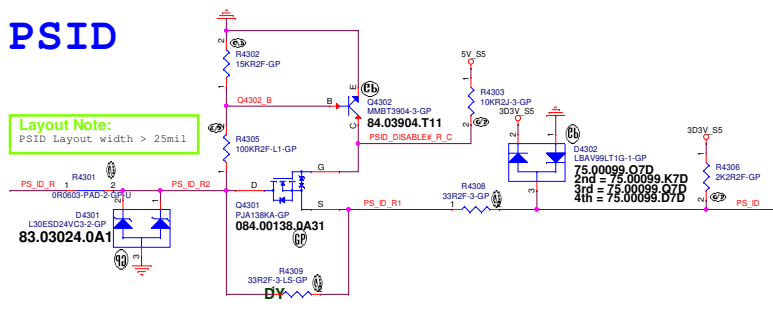
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (RSVD)			
Size A4	Document Number Bandon / NorthBay 13"		Rev X00
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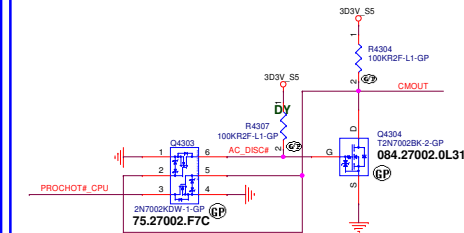
Main Func = DCIN & BATT Com

	[24]	PS_ID	<<<	_____
[3,24,44,6]		PROCHOT_CPU	<<<	_____
	[44]	CMOUT	<<<	_____
	[24,44]	AC_DIS	>>>	_____
	[24]	DC2N_EN	>>>	_____
[24,44]		PBAT_CHARGER_SMBCLK	<<<	_____
[24,44]		PBAT_CHARGER_SMBDAT	<<<	_____
	[24,44]	PBAT_PRES#	<<<	_____
[74]		PWR_VBUS_OVP_OUT_R	>>>	_____
	[24,74]	AC_DIS#	<<<	_____
[24,44,74]		HW_ACAVIN_NB	<<<	_____
	[24,74]	VBUS1_ECON	<<<	_____

PSID

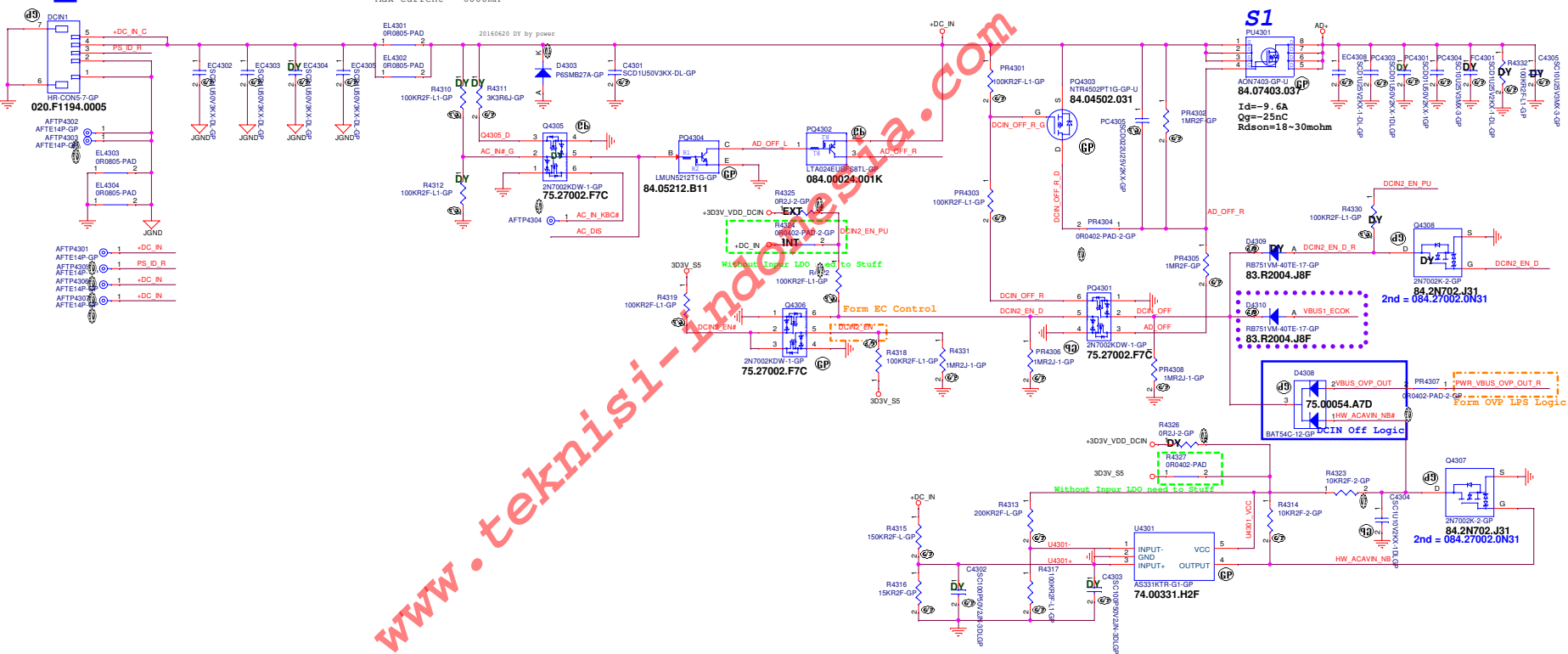


AC Disconnect Latch

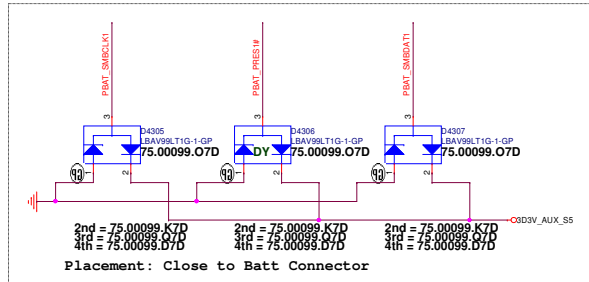
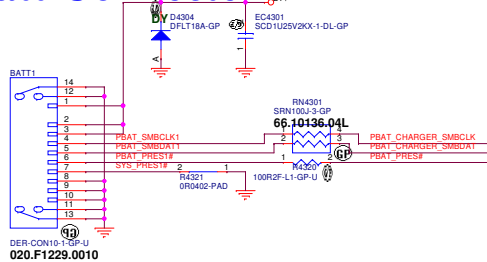


DC_IN

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA



Batt Connector



Main Func = Power_Charger

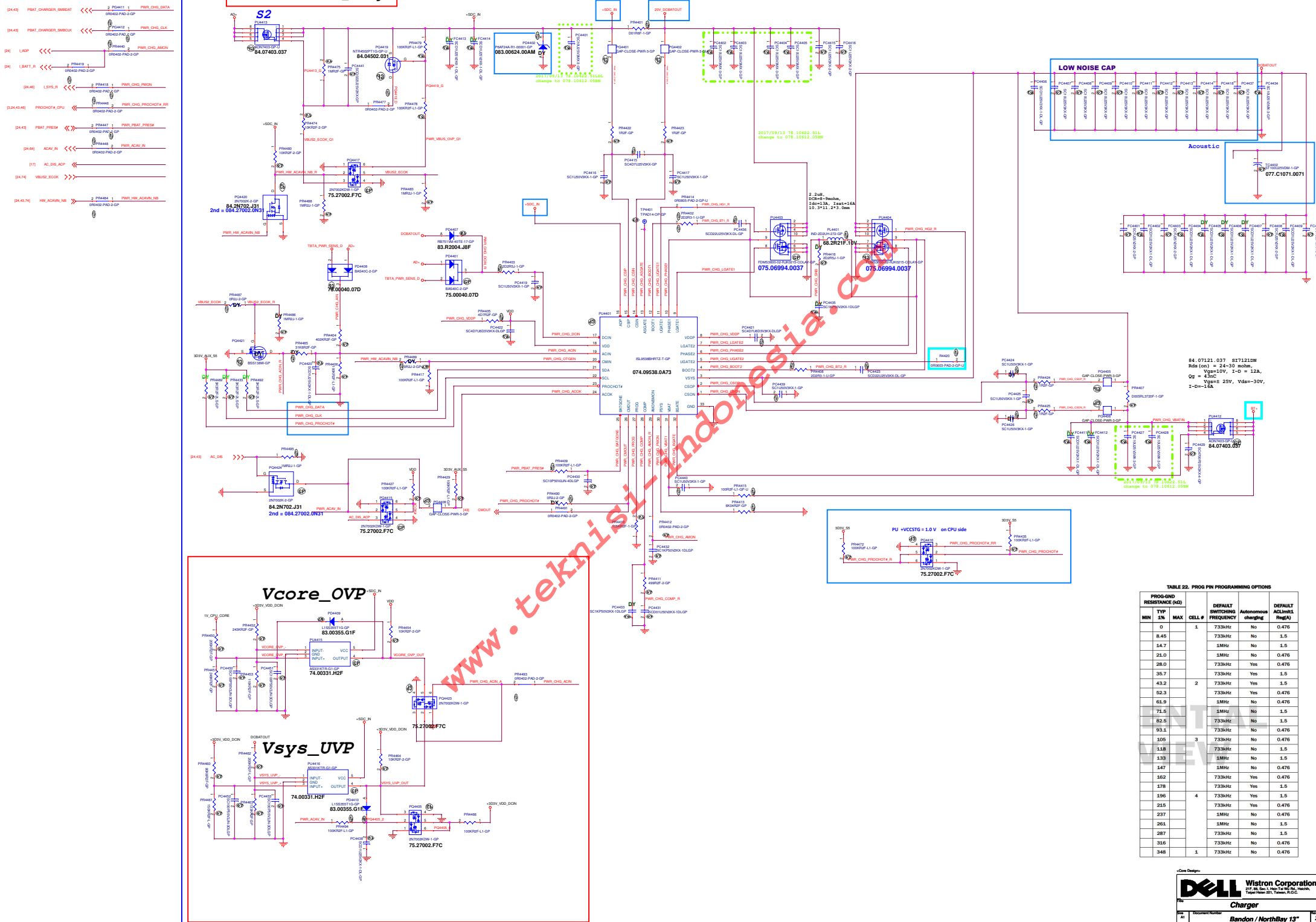


TABLE 22. PROG PIN PROGRAMMING OPTIONS

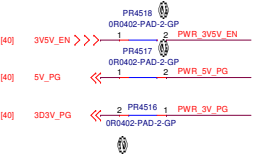
PROG-RESISTANCE (Ω)	TYP	1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit Reg(A)
0				1	733kHz	No	0.476
8.45					733kHz	No	1.5
14.7					1MHz	No	1.5
21.0					1MHz	No	0.476
28.0					733kHz	Yes	0.476
35.7					733kHz	Yes	1.5
43.2				2	733kHz	Yes	1.5
52.3					733kHz	Yes	0.476
61.9					1MHz	No	0.476
71.6					1MHz	No	1.5
82.5					733kHz	No	1.5
93.1					733kHz	No	0.476
105				3	733kHz	No	0.476
118					733kHz	No	1.5
133					1MHz	No	1.5
147					1MHz	No	0.476
162					733kHz	Yes	0.476
178					733kHz	Yes	1.5
196				4	733kHz	Yes	1.5
215					733kHz	Yes	0.476
237					1MHz	No	0.476
261					1MHz	No	1.5
287					733kHz	No	1.5
316					733kHz	No	0.476
348				1	733kHz	No	0.476

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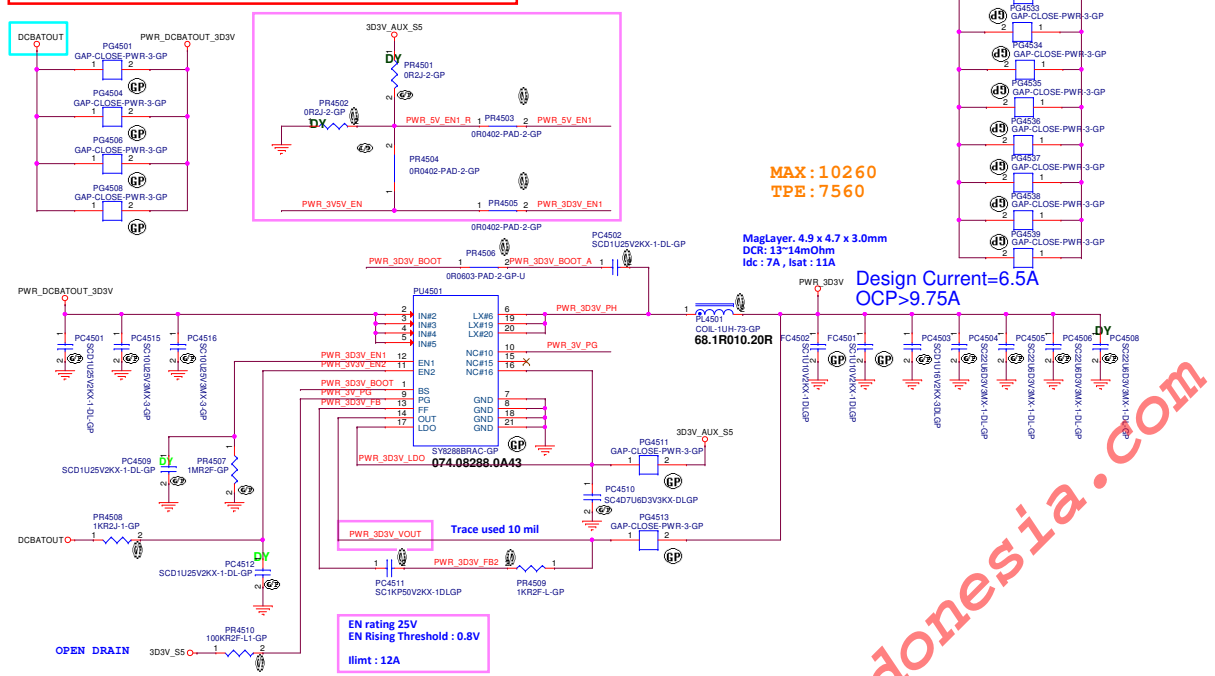
DELL Wistron Corporation
 21F, 8B, 5C, 1, Hsin-Fu Rd, Hsin-Fu, Taiwan
 Taipei, Taiwan 111, Taiwan, R.O.C.

Charger
 Document Number
 Bandon / North Bay 13" X100
 Rev. 1.00, February 13, 2013

OFFPAGE



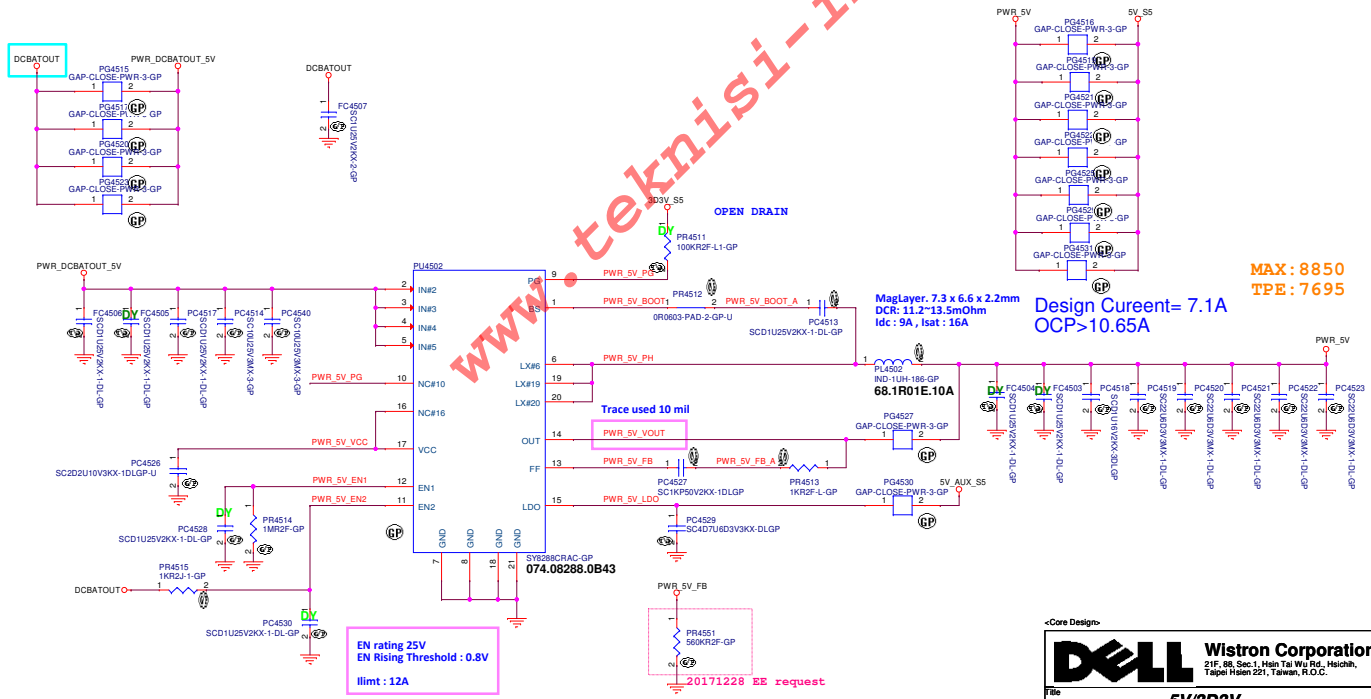
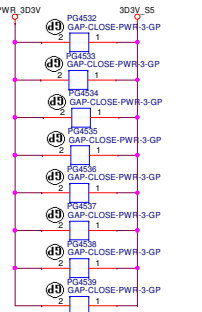
Main Func = Power_System 5V/3D3V



MAX: 10260
TPE: 7560

MagLayer: 4.9 x 4.7 x 3.0mm
DCR: 13~14mOhm
Idc: 7A, Isat: 11A

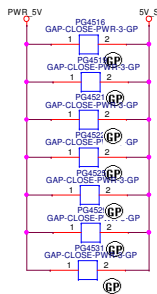
Design Current=6.5A
OCP>9.75A



MAX: 8850
TPE: 7695

MagLayer: 7.3 x 6.6 x 2.2mm
DCR: 11.2~13.5mOhm
Idc: 9A, Isat: 16A

Design Current= 7.1A
OCP>10.65A



Core Design

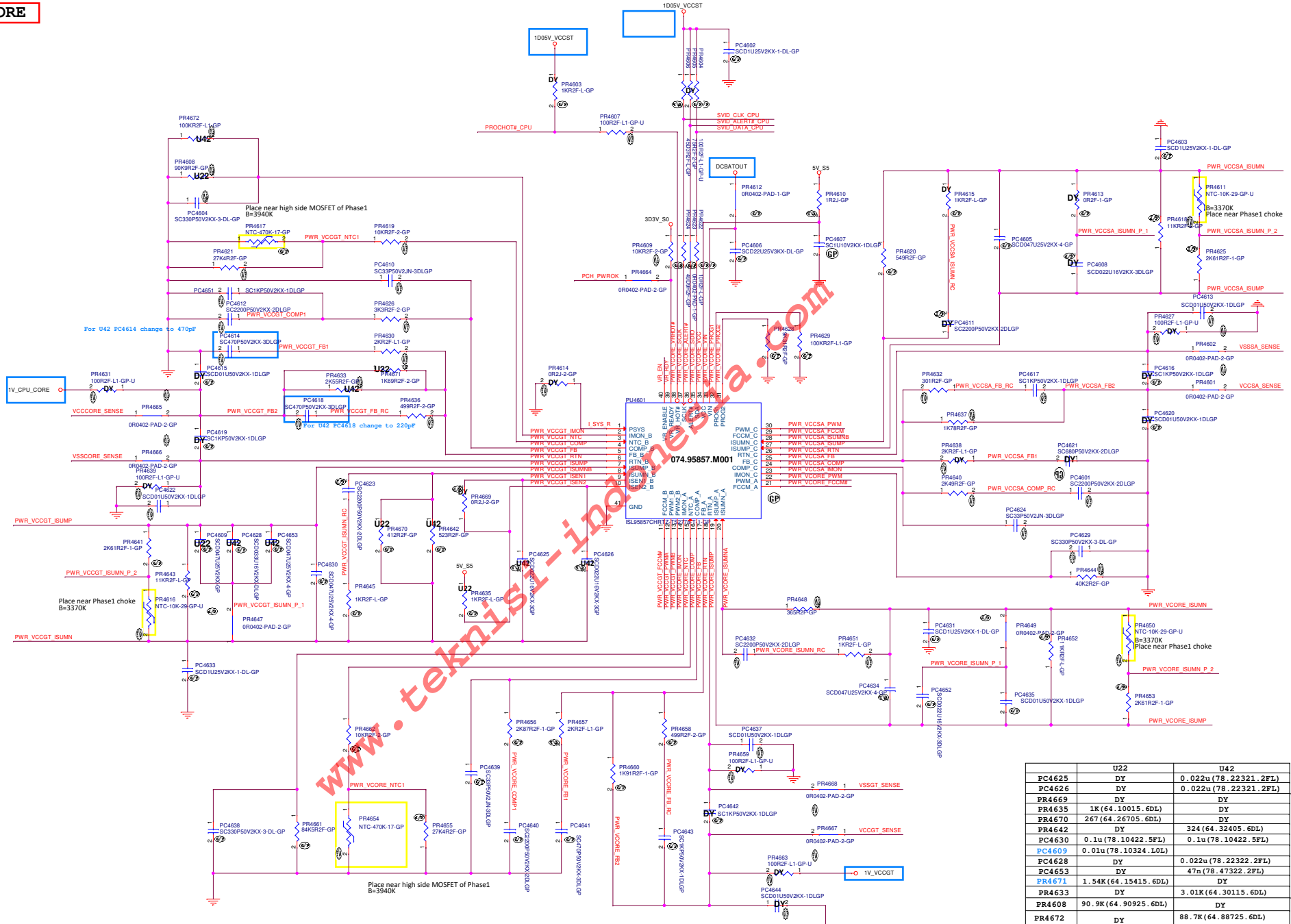
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

File: 5V/3D3V

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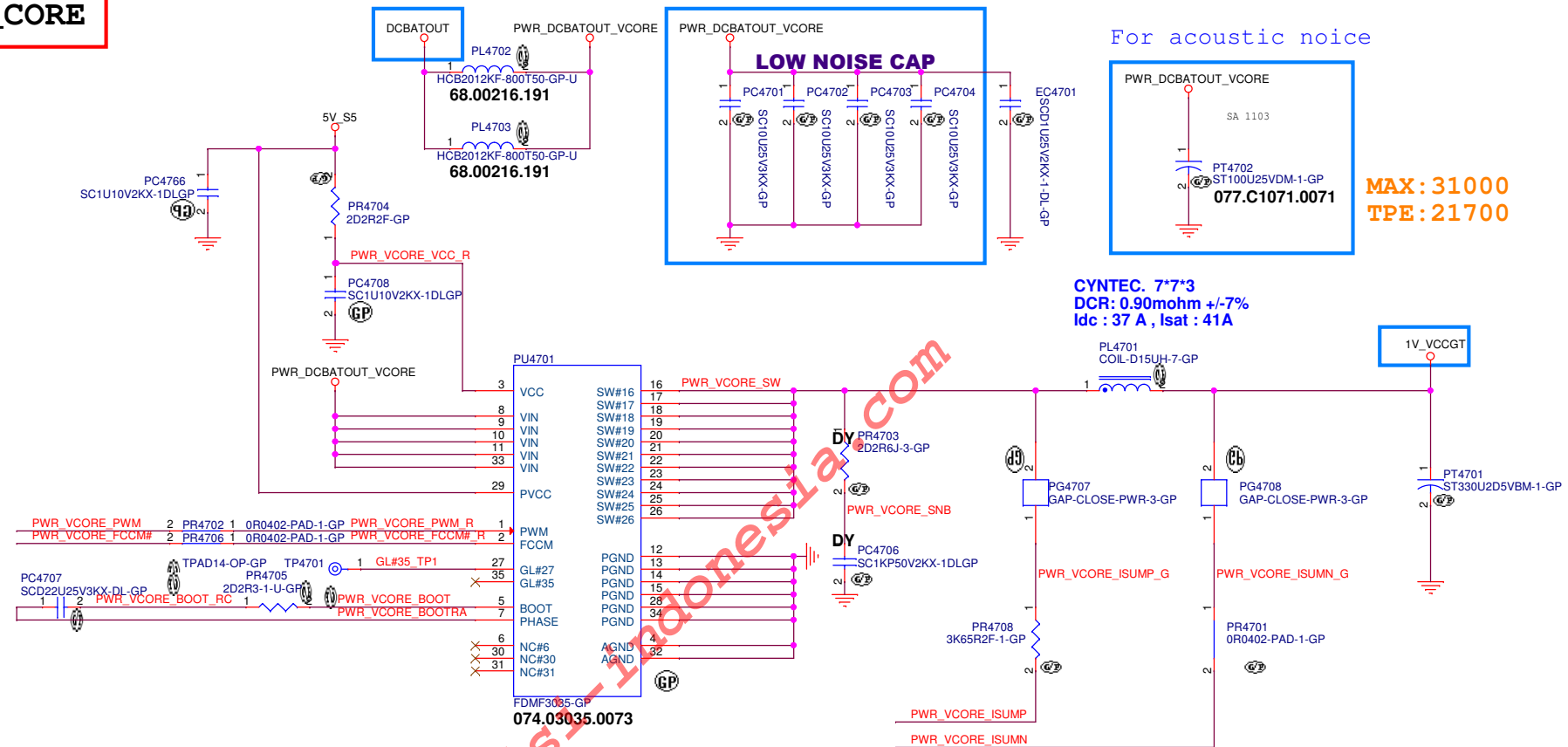
[7]	SWD_CLK_CPU	<<<
[7]	SWD_ALERT1_CPU	<<<
[7]	SWD_DATA_CPU	<<<
[7]	VCCOCC Sense	<<<
[7]	VSSOCC Sense	<<<
[48]	PWR_VCCGT_ISUMP	>>>
[48]	PWR_VCCGT_ISUMIN	>>>
[48]	PWR_VCCGT_ISEN1	>>>
[48]	PWR_VCCGT_ISEN2	>>>
[8]	VSSGT Sense	<<<
[8]	VCCGT Sense	<<<
[47]	PWR_VCORE_ISUMIN	>>>
[47]	PWR_VCORE_ISUMP	>>>
[50]	PWR_VCCSA_ISUMIN	>>>
[50]	PWR_VCCSA_ISUMP	>>>
[8]	VSSSA Sense	<<<
[8]	VCCSA Sense	<<<
[48]	PWR_VCCGT_FCCM	>>>
[48]	PWR_VCCGT_FWMA	>>>
[48]	PWR_VCCGT_FWMB	>>>
[50]	PWR_VCCSA_PWM	>>>
[50]	PWR_VCCSA_FCCM	>>>
[47]	PWR_VCORE_PWM	>>>
[47]	PWR_VCORE_FCCM	>>>
[34]	VR_EN	>>>
[32,43,44]	PROCHOT_CPU	<<<
[17]	PCH_PWROK	<<<
[24,44]	1 SYS R	<<<



	U22	U42
PC4625	DY	0.022u(78.22321.2FL)
PC4626	DY	0.022u(78.22321.2FL)
PR4669	DY	DY
PR4635	1K(64.10015.6DL)	DY
PR4670	267(64.26705.6DL)	DY
PR4642	DY	324(64.32405.6DL)
PC4630	0.1u(78.10422.5FL)	0.1u(78.10422.5FL)
PC4609	0.01u(78.10324.1DL)	
PC4628	DY	0.022u(78.22322.2FL)
PC4653	DY	47n(78.47322.2FL)
PR4671	1.54K(64.15415.6DL)	DY
PR4633	DY	3.01K(64.30115.6DL)
PR4608	90.9K(64.90925.6DL)	DY
PR4672	DY	88.7K(64.88725.6DL)

Main Func = CPU_CORE

```
[46] PWR_VCORE_PWM >>>
[46] PWR_VCORE_FCCM# >>>
[46] PWR_VCORE_ISUMP <<<
[46] PWR_VCORE_ISUMN <<<
```



<Core Design>



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Title

ISL95859C_CPU_VCORE(2/3)

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[46]	PWR_VCCGT_PWMA	»»
[46]	PWR_VCCGT_FCCM#	»»
[46]	PWR_VCCGT_ISEN1	««
[46]	PWR_VCCGT_ISUMP	««
[46]	PWR_VCCGT_ISUMN	««
[46]	PWR_VCCGT_ISEN2	««
[46]	PWR_VCCGT_PWMB	»»



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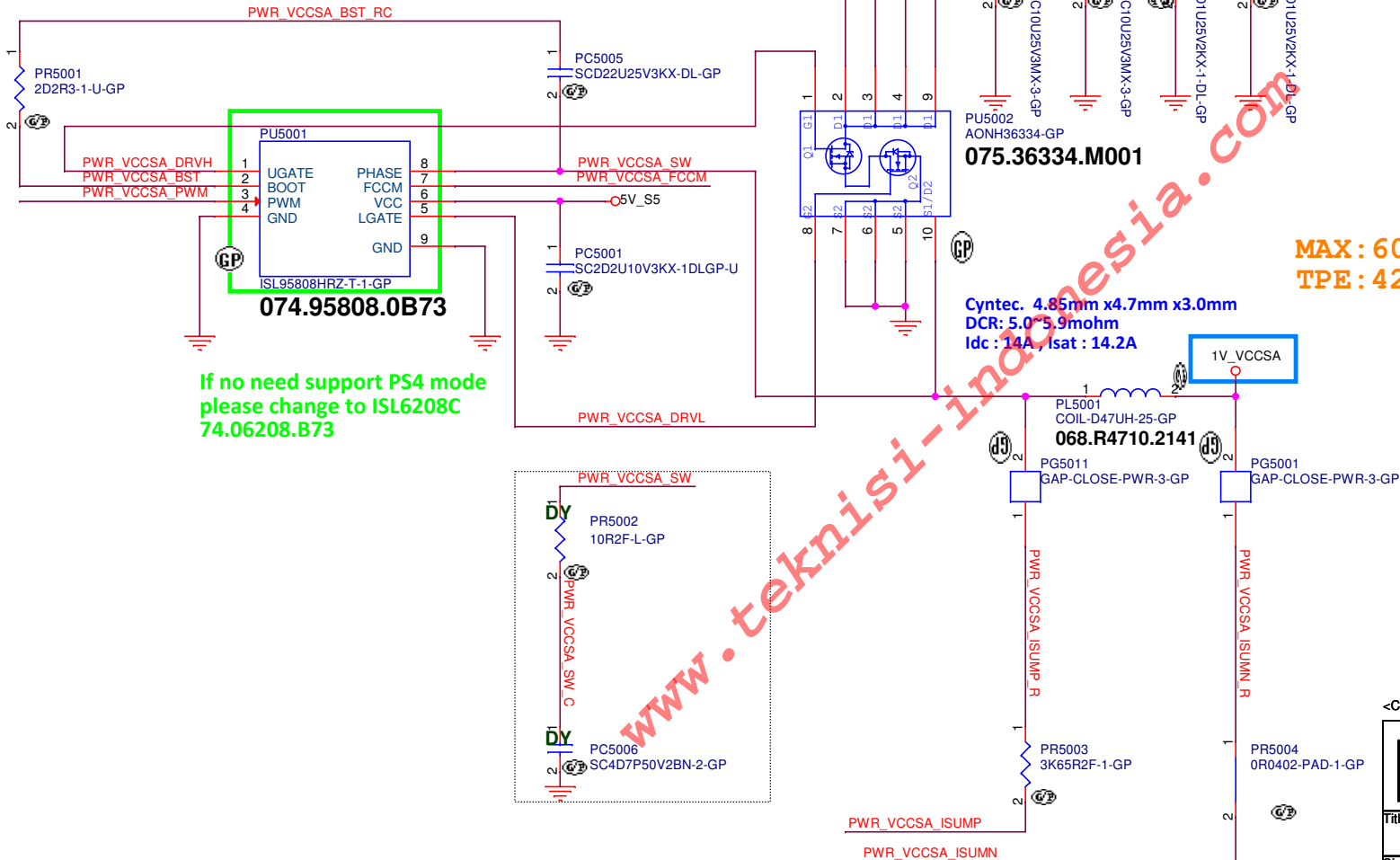
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title NCP81210MN_CPU_VCCGTUS					
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Main Func = CPU_VCCSA

[46] PWR_VCCSA_PWM >>>—
[46] PWR_VCCSA_ISUMP <<<—
[46] PWR_VCCSA_ISUMN <<<—
[46] PWR_VCCSA_FCCM >>>—



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Title		VCCSA	
Size	Document Number	Rev	
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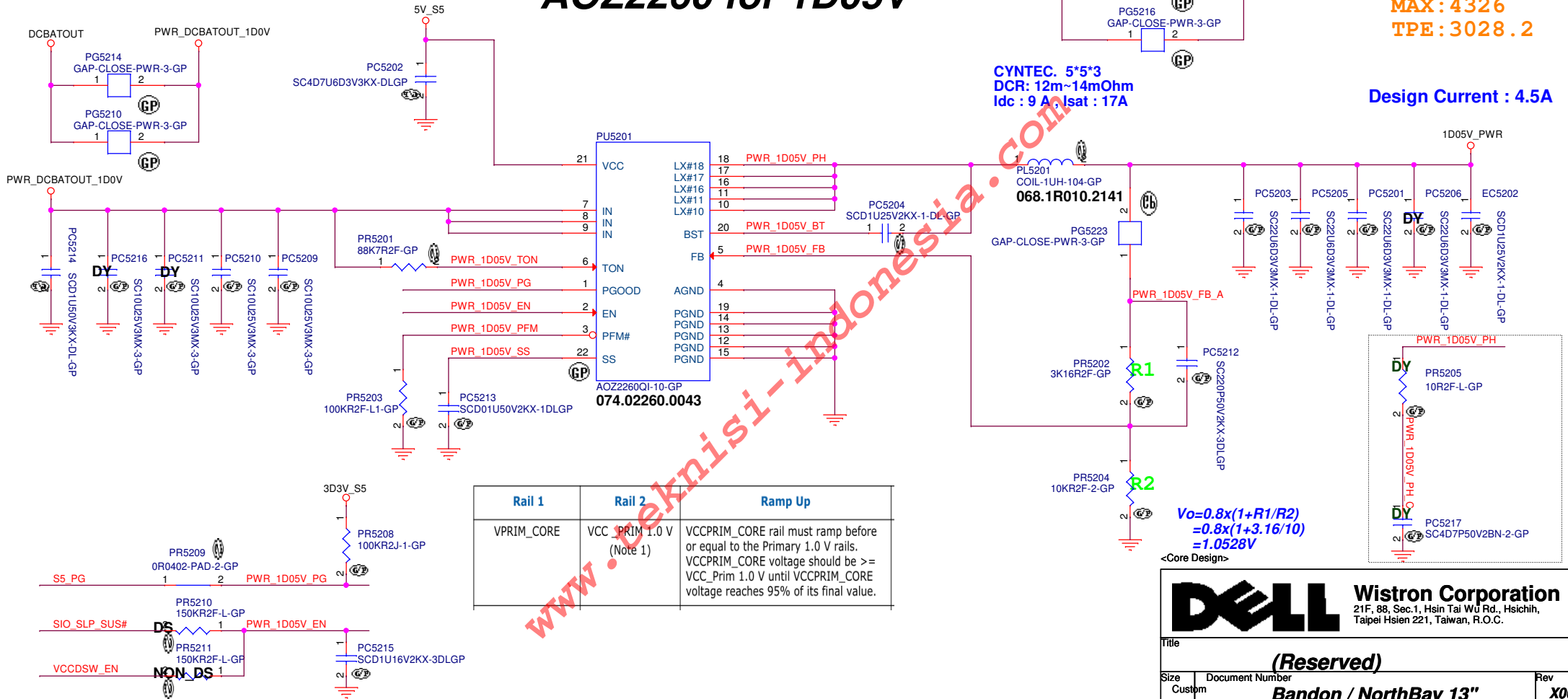
SSID = PWR.Plane.Regulator_1D05V

[24,53,54] S5_PG <<<—

[17,24,40,53,54] SIO_SLP_SUS# >>>—

[24,40,53,54] VCCDSW_EN >>>—

AOZ2260 for 1D05V



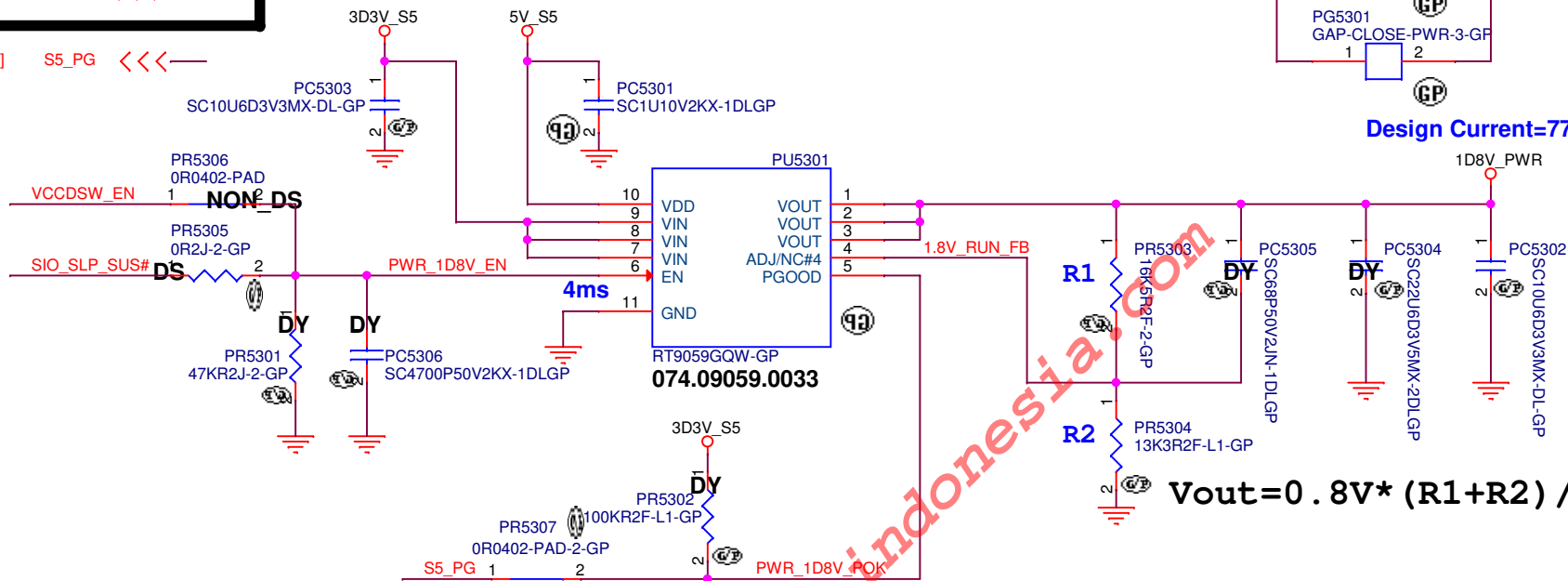
Main Func = 1D8V

APL5934 for 1D8V_S5

MAX: 917
TPE: 641.9

Design Current=770mA

$$V_{out} = 0.8V * (R1 + R2) / R2$$



<Core Design>



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Title

(Reserved)

Size
A4

Document Number

Bandon / NorthBay 13"

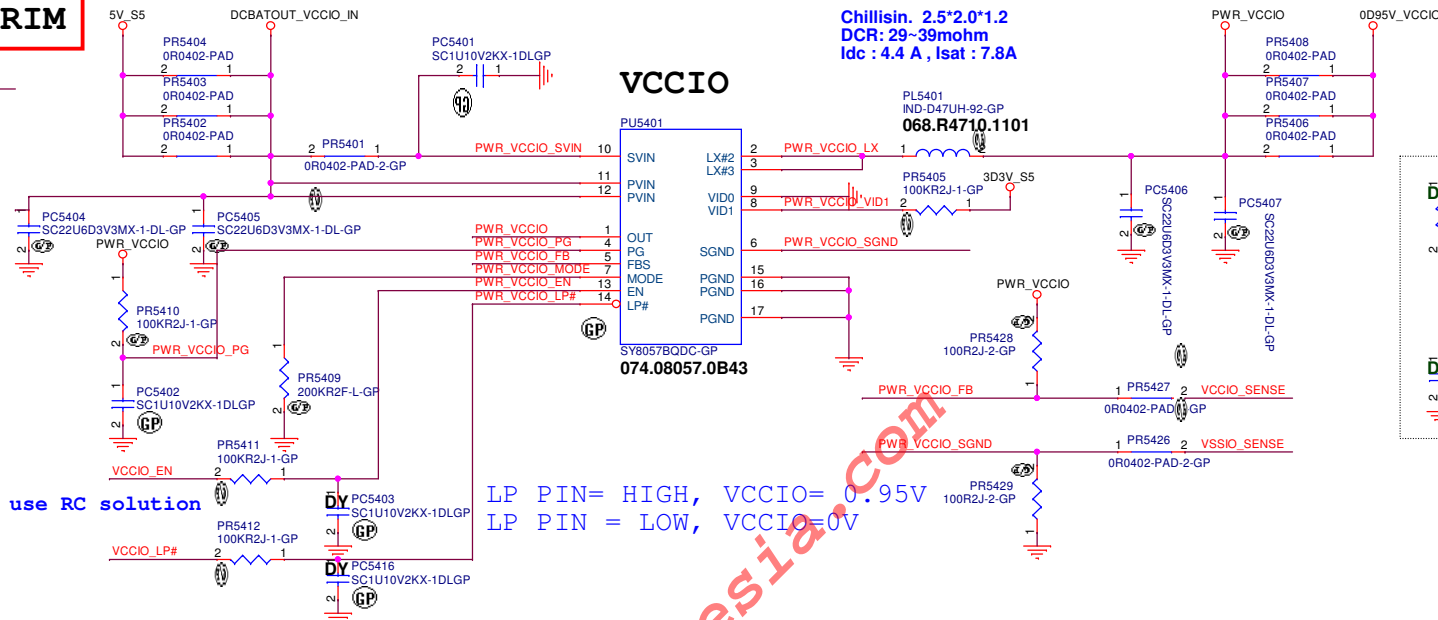
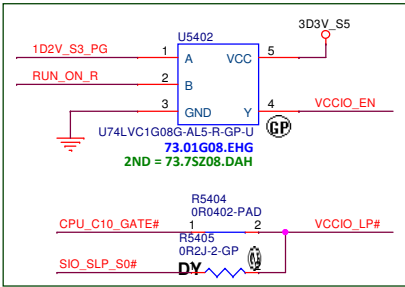
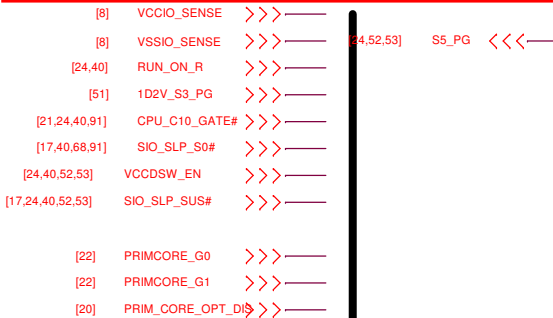
Rev

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Main Func = VCCIO / VCCPRIM

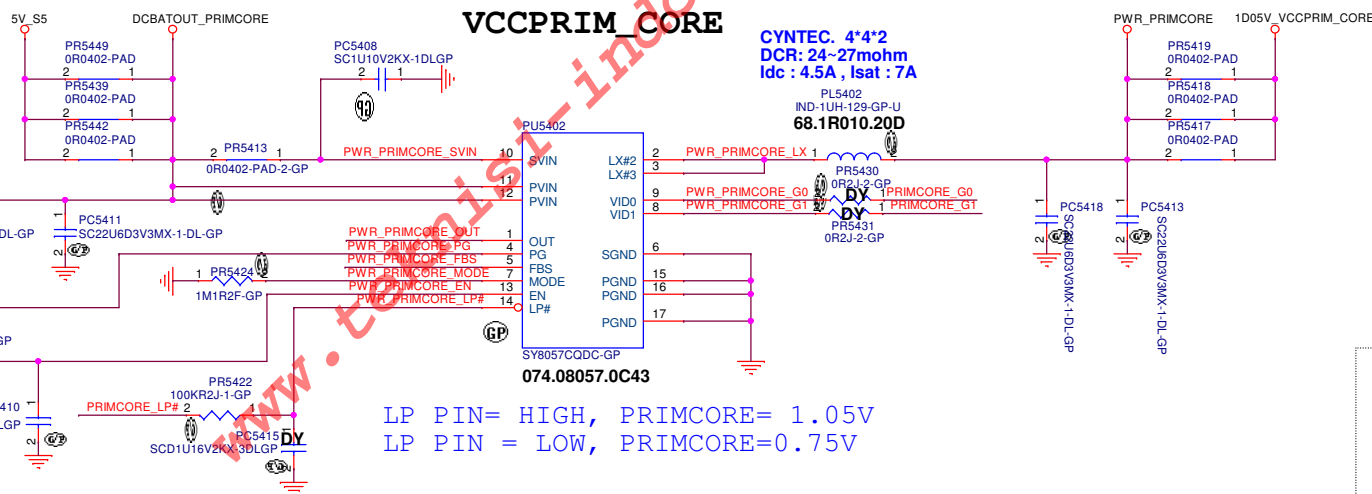


MAX: 1000
TPE: 700

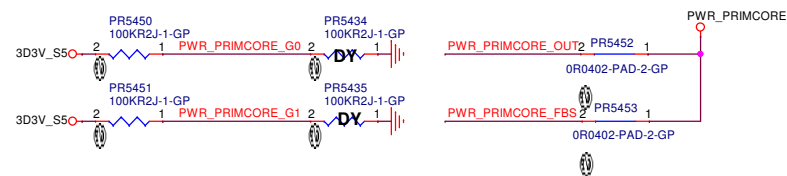
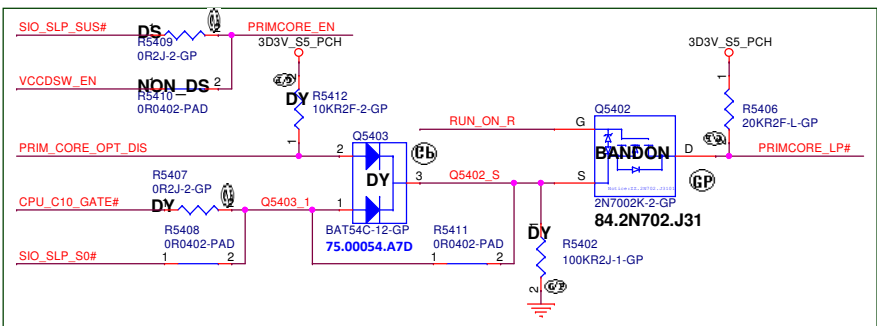
EV2 test use RC solution

LP PIN= HIGH, VCCIO= 0.95V
LP PIN = LOW, VCCIO=0V

MAX: 4260
TPE: 2982



LP PIN= HIGH, PRIMCORE= 1.05V
LP PIN = LOW, PRIMCORE=0.75V



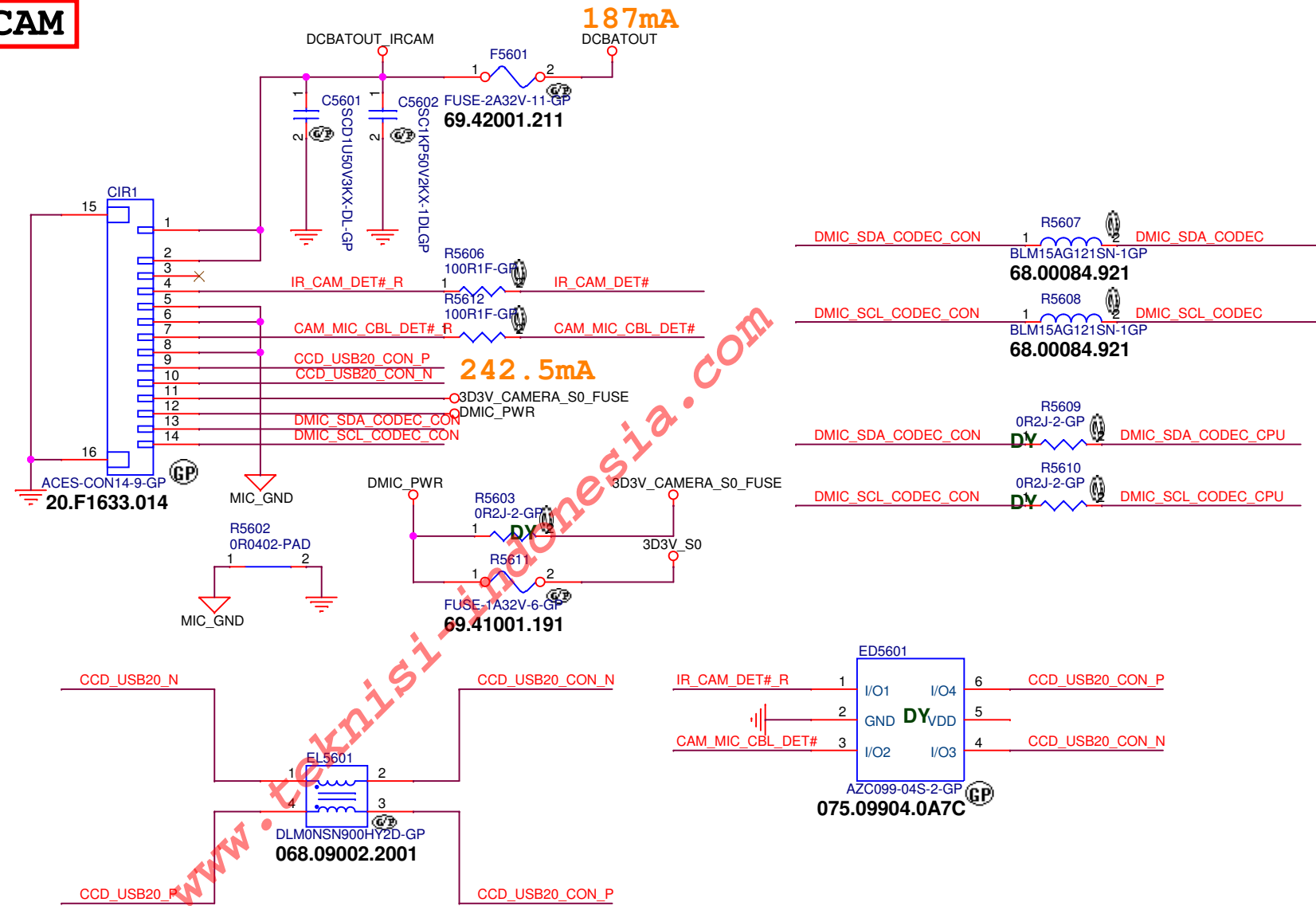
<Core Design>

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Main Func = IR CAM

CAMERA

[16]	CCD_USB20_N	<<<<
[16]	CCD_USB20_P	<<<<
[27]	DMIC_SDA_CODEEC	<<<<
[27]	DMIC_SCL_CODEEC	<<<<
[20]	IR_CAM_DET#	<<<<
[19]	CAM_MIC_CBL_DET#	<<<<
[19]	DMIC_SDA_CODEEC_CPU	<<<<
[19]	DMIC_SCL_CODEEC_CPU	<<<<



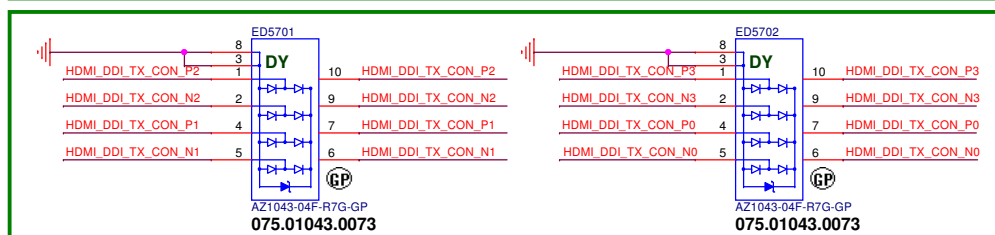
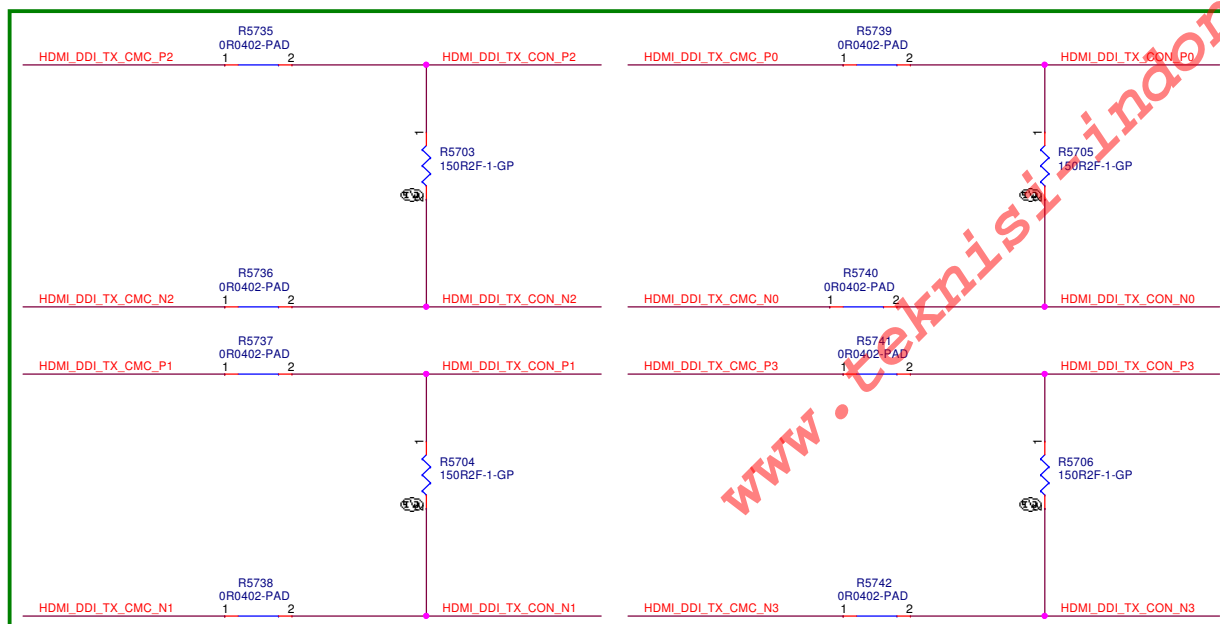
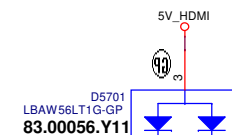
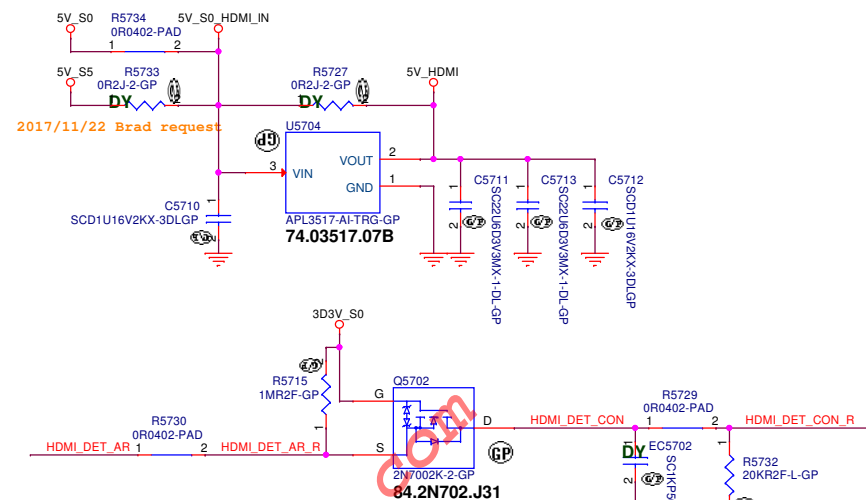
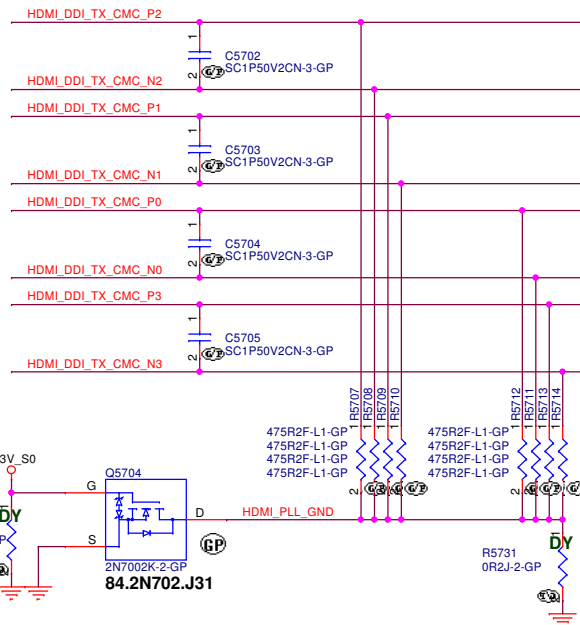
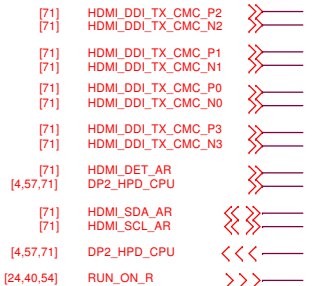
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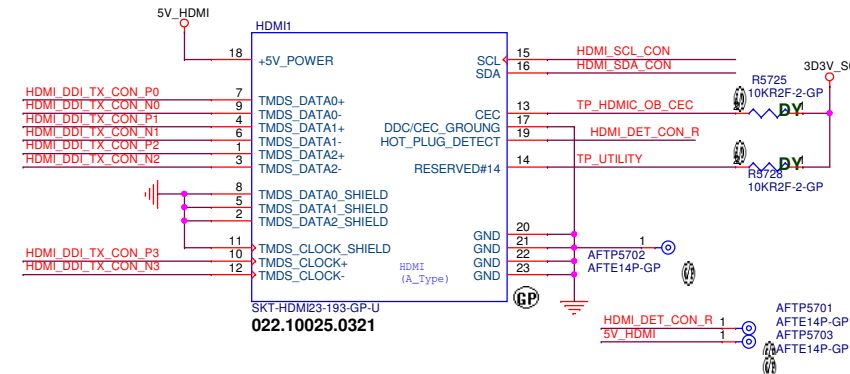
Title: **Display (LCD/Inverter)**

Size: A4	Document Number: Bandon / NorthBay 13"	Rev: X00
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Main Func = HDMI



HDMI CONNECTOR



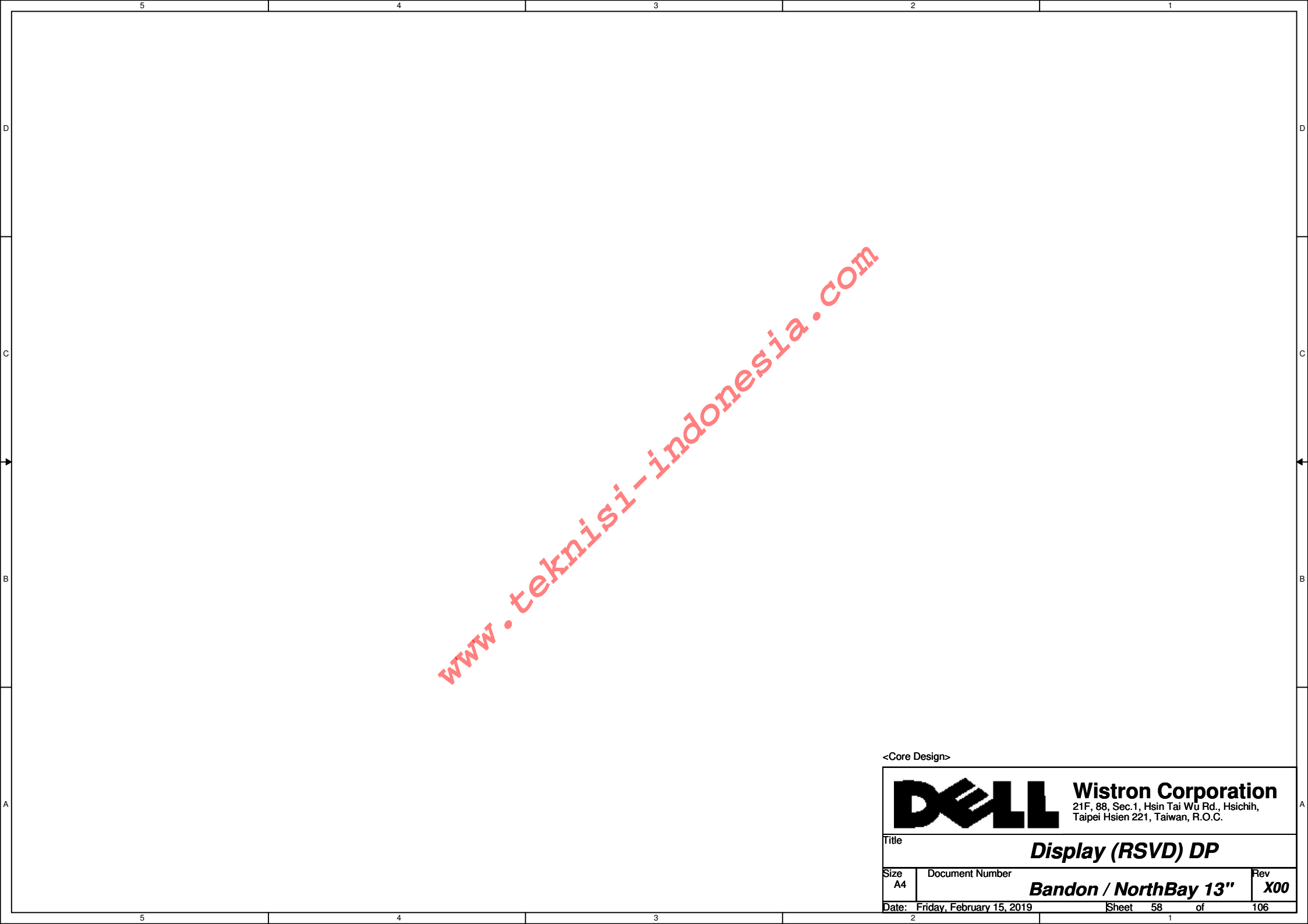
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Title **Display (HDMI Level Shifter/Conn)**


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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Display (RSVD) DP		
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<Core Design>

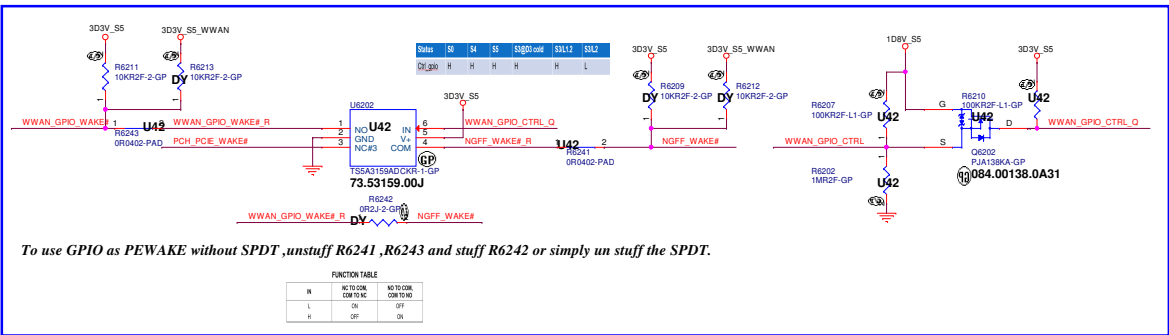
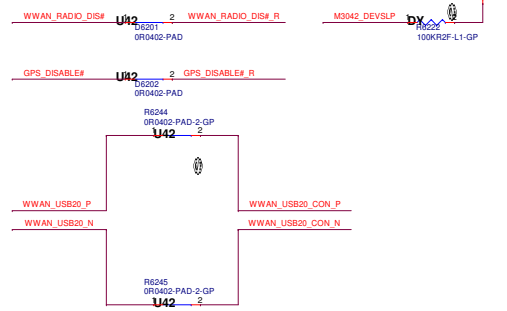
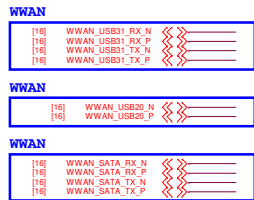
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Display (RSVD) DVI		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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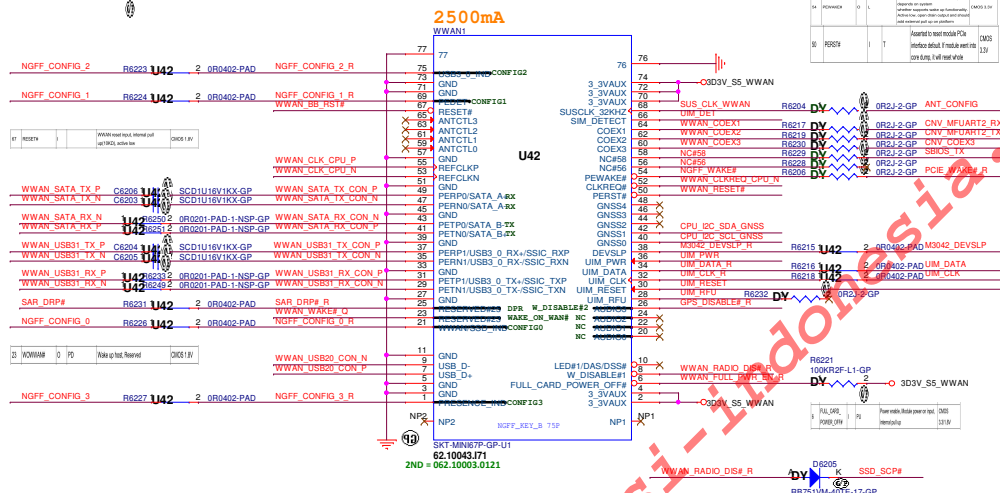
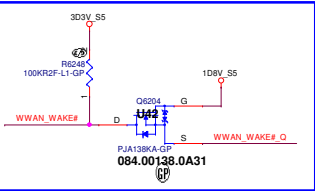
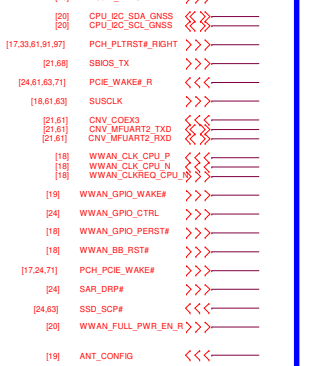
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title INT IO (RSVD)(HDD)		
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$$NGFF(WWAN/SSD)$$


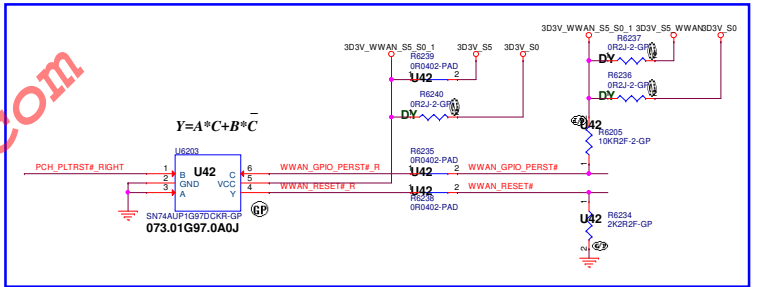
To use GPIO as PEWAKE without SPDT ,unstuff R6241 ,R6243 and stuff R6242 or simply un stuff the SPDT

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON



54	PCWATCHDOG	O	L	<p>Assorted to enable up system and disable PCIE link V1.2 to V2.8, depending on system</p> <p>Whether supports wake up functionality, whether it is upper layer control and should enable external pull up on platform</p>	CMOS 1.5V
56	PERST#	I	T	<p>Asserted to reset module PCIe interface before it module went into core dump, it will reset whole</p>	CMOS 1.5V

$$Y=A * C+B * \bar{C}$$



STATE#	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M0042_POEIR_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-POE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-POE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

The M.2 module configuration as the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	GND	GND	NC	WWAN-USB3.1, PCIe Gen1	0

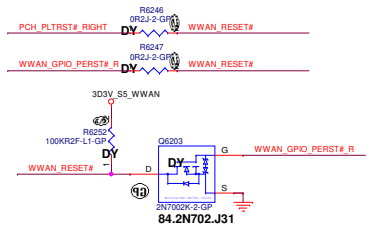


Figure 3-5 Timing Control for Start-up

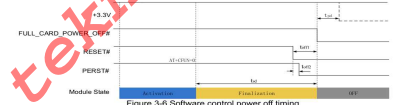
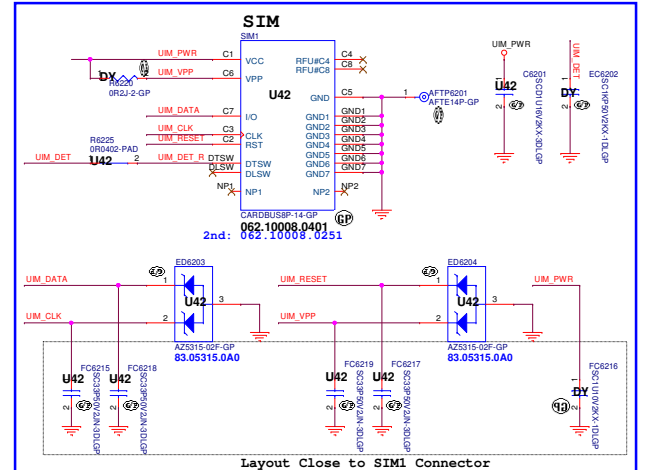


Figure 3-6 Software control power off timing

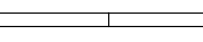
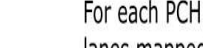
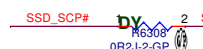
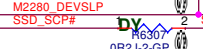
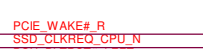
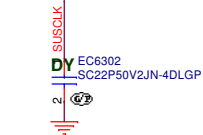
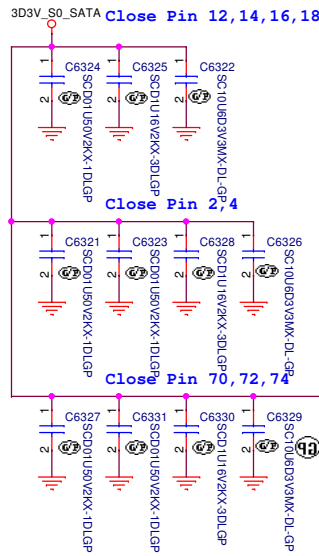
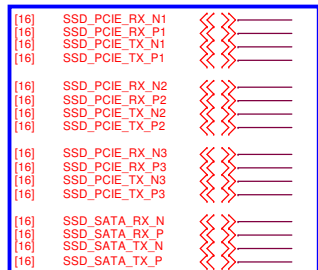
Index	Minimum	Typical	Notes	Index	Minimum	Typical	Maxim	Notes
t _{sr}	-	-	+3.3V power supply rises time. If power supply always reaches there is no t _{sr}	t _{sd}	10ms	100ms	-	+3.3V power supply goes down time. If power supply is always on, there is no t _{sd}
t _{on1}	10ms	30ms	If the RESET# has a residual voltage, then 30ms is the primary	t _{on2}	10ms	30ms	-	RESET# should asserted before FULL_CARD_POWER_OFF#
t _{on2}	10ms	30ms	PERST# should de-asserted after FULL_CARD_POWER_OFF#	t _{off2}	0ms	30ms	t _{off1}	PERST# should asserted after RESET#



Layout Close to SIM1 Connector

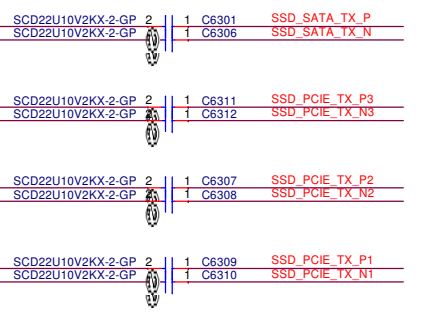
Main Func = m.2 SSD

SSD



PEDET	0	Host I/F Indication; To be grounded for SATA, No Connect for PCIe	OV/NC
L		SATA	
H		PCIe	

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

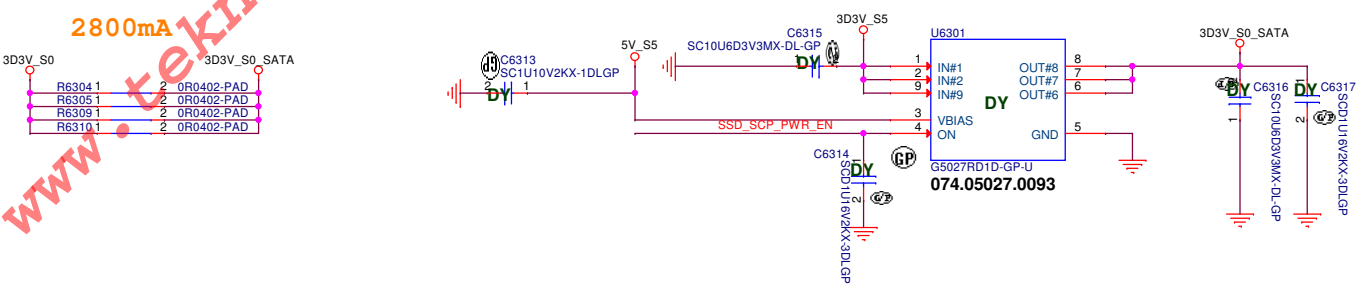


74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	N/C	67
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKN	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
44	N/C	GND	45
42	N/C	PERp0/SATA-B-	43
40	N/C	PERn0/SATA-B+	41
38	DEVSLP (O)	GND	39
36	N/C	PETp1	37
34	N/C	PETn1	35
32	N/C	GND	33
30	N/C	PERp1	31
28	N/C	PERn1	29
26	N/C	GND	27
24	N/C	PETp2	25
22	N/C	PETn2	23
20	N/C	GND	21
18	3.3V	PERp2	19
16	3.3V	PERn2	17
14	3.3V	GND	15
12	3.3V	PETp3	13
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	PETn3	11
8	N/C	GND	9
6	N/C	PERp3	7
4	3.3V	PERn3	5
2	3.3V	GND	3
		GND	1

6.5.4.6

PCH PCI Express* Controller Lane Reversal

For each PCH PCIe* Controller we support end-to-end lane reversal across the four lanes mapped to a controller for the following two motherboard PCIe* configurations



<Core Design>

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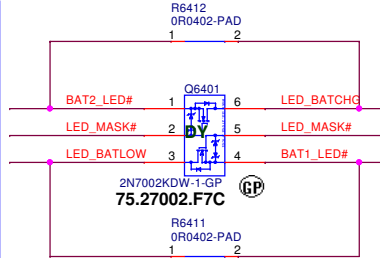
Title: **INT IO (SSD M.2/ eMMC)**

Size A3 Document Number: **Bandon / NorthBay 13"** Rev: **X00**

Date: Friday, February 15, 2019 Sheet 63 of 106

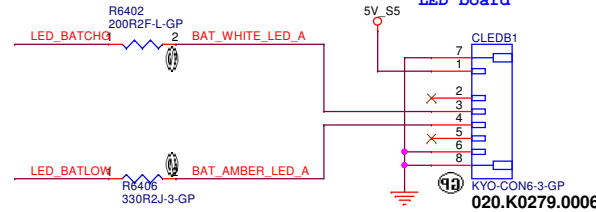
Main Func = LED/HALL/Button

[24] BAT2_LED# >>>
 [24] BAT1_LED# >>>
 [24,32] LED_MASK# >>>
 [24,66,68] KBC_PWRBTN# <<<
 [24,55,67] LID_CL_SIO#_R <<<
 [24,67] LID_CL_SIO_TAB#_R >>>
 [24] BREATH_LED# <<<
 [24,92] FPR_DET# >>>
 [24] M_BIST >>>
 [24,44] ACAV_IN >>>
 [17,24,99] RSMRST#_KBC >>>

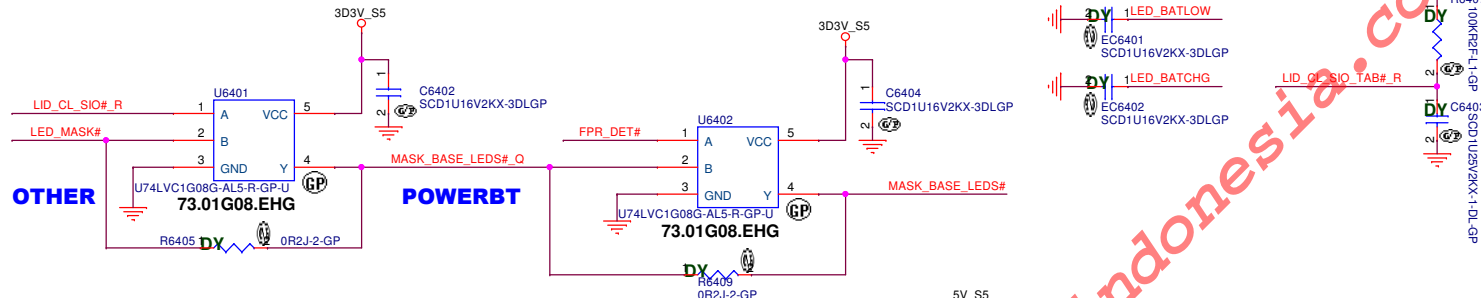
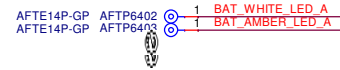


Stealth mode

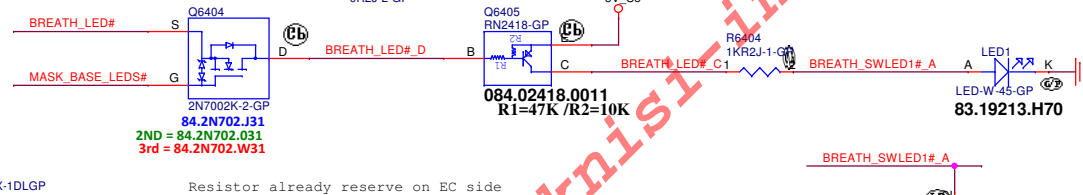
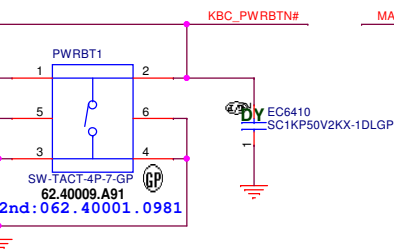
Battery LED2(White LED) LOW acted from KBC GPIO



Battery LED1(Orange LED) LOW acted from KBC GPIO

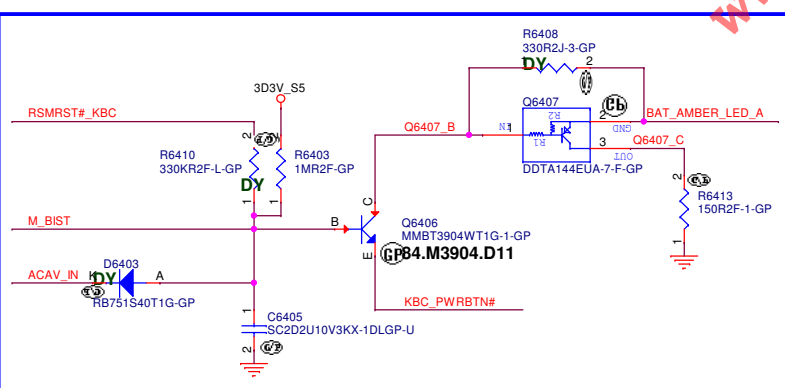


POWER BUTTON



Power LED LOW acted from KBC GPIO

M-BIST



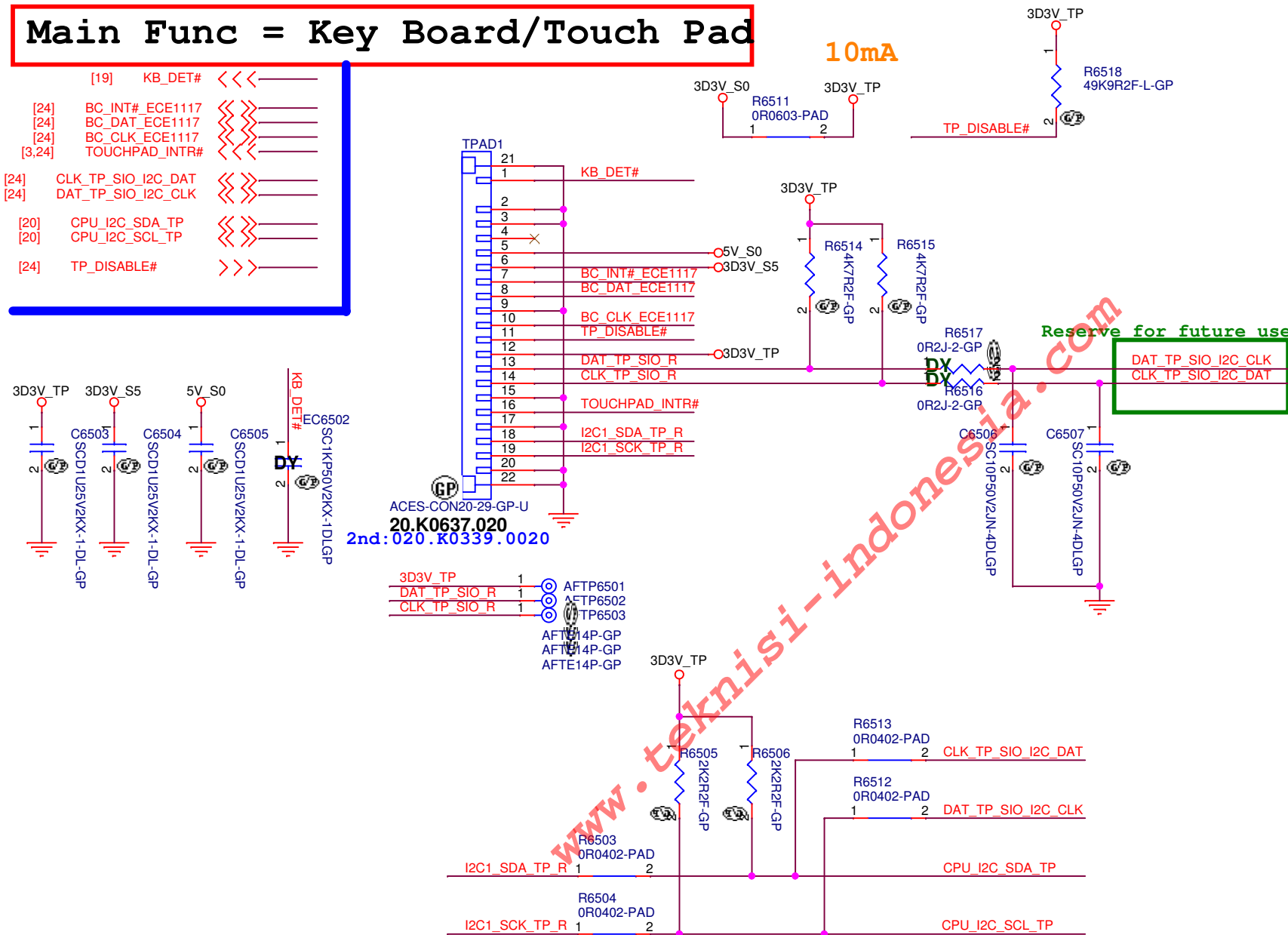
<Core Design>

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Title LED / Button / Power Button		
Size Custom	Document Number Bandon / NorthBay 13"	Rev X00
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Main Func = Key Board/Touch Pad

[19]	KB_DET#	<<<
[24]	BC_INT#_ECE1117	<<<
[24]	BC_DAT#_ECE1117	<<<
[24]	BC_CLK#_ECE1117	<<<
[3,24]	TOUCHPAD_INTR#	<<<
[24]	CLK_TP_SIO_I2C_DAT	<<<
[24]	DAT_TP_SIO_I2C_CLK	<<<
[20]	CPU_I2C_SDA_TP	<<<
[20]	CPU_I2C_SCL_TP	<<<
[24]	TP_DISABLE#	>>>



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Title

INT IO (KB/TP)

Size
A4

Document Number

Bandon / NorthBay 13"

Rev
X00

Date: Friday, February 15, 2019

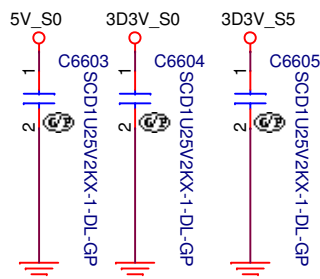
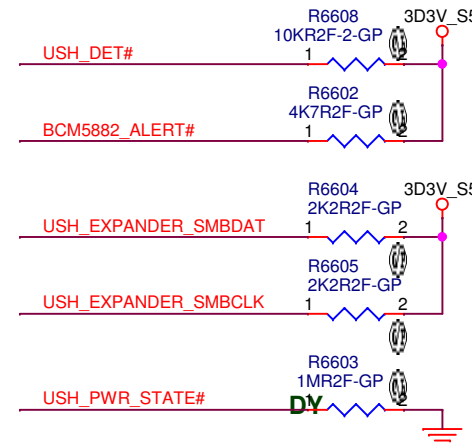
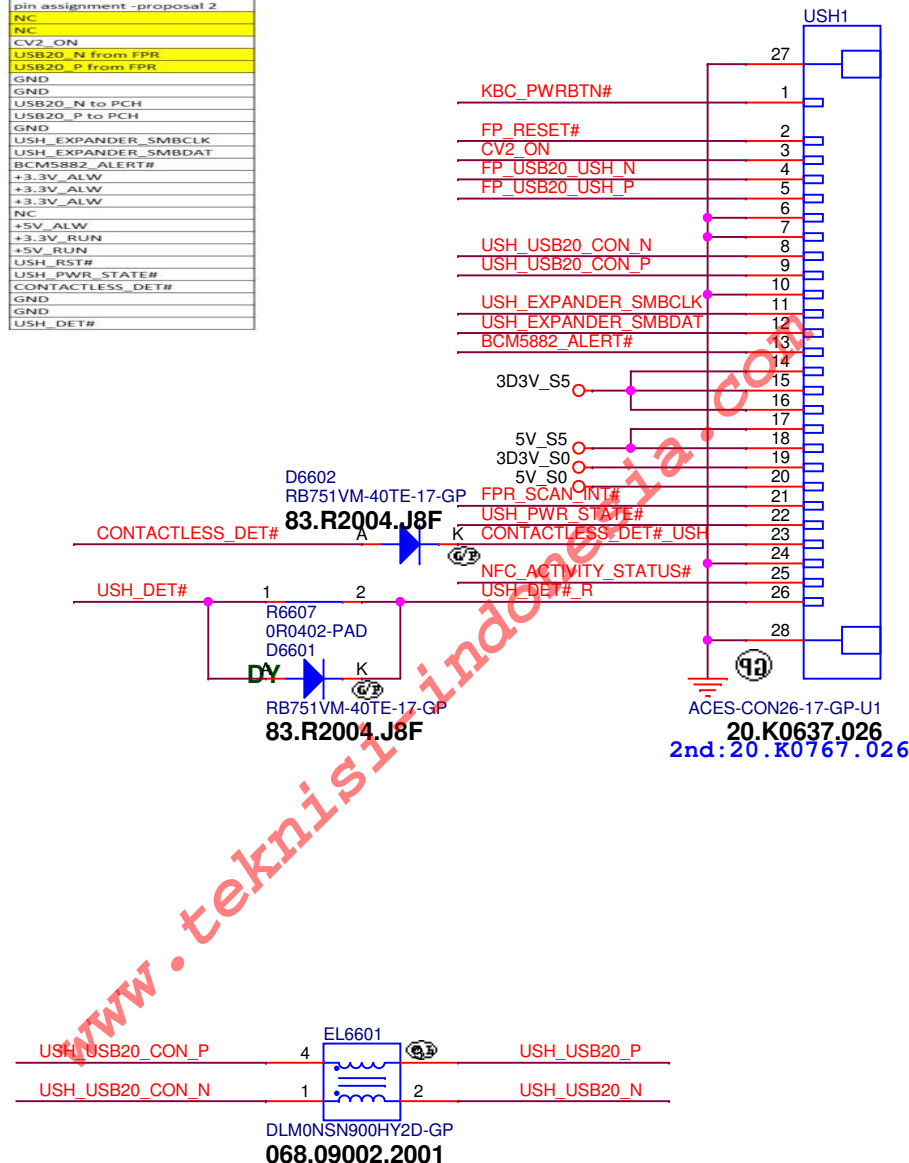
Sheet 65 of 106

Main Func = USH BD

USH

[16]	USH_USB20_N	<<>>	
[16]	USH_USB20_P	<<>>	
[24]	CV2_ON	>>>	
[24,69]	USH_EXPANDER_SMBCLK	<<>>	
[24,69]	USH_EXPANDER_SMBDAT	<<>>	
[24]	BCM5882_ALERT#	>>>	
[24]	USH_PWR_STATE#	<<<	
[19]	CONTACTLESS_DET#	<<<	
[24]	USH_DET#	<<<	
[16,92]	FP_USB20_N	<<>>	
[16,92]	FP_USB20_P	<<>>	
[92]	FP_USB20_USH_N	<<>>	
[92]	FP_USB20_USH_P	<<>>	
[24]	NFC_ACTIVITY_STATUS#	<<<	
[92]	FP_RESET#	<<<	
[24,92]	FPR_SCAN_INT#	>>>	
[24,64,68]	KBC_PWRBTN#	>>>	

CV3 module
pin assignment - proposal 2
NC
NC
CV2_ON
USB20_N from FPR
USB20_P from FPR
GND
GND
USB20_N to PCH
USB20_P to PCH
GND
USH_EXPANDER_SMBCLK
USH_EXPANDER_SMBDAT
BCM5882_ALERT#
+3.3V_ALW
+3.3V_ALW
+3.3V_ALW
NC
+5V_ALW
+3.3V_RUN
+5V_RUN
USH_RST#
USH_PWR_STATE#
CONTACTLESS_DET#
GND
GND
USH_DET#



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Title **IO Board Conn (USH)**

Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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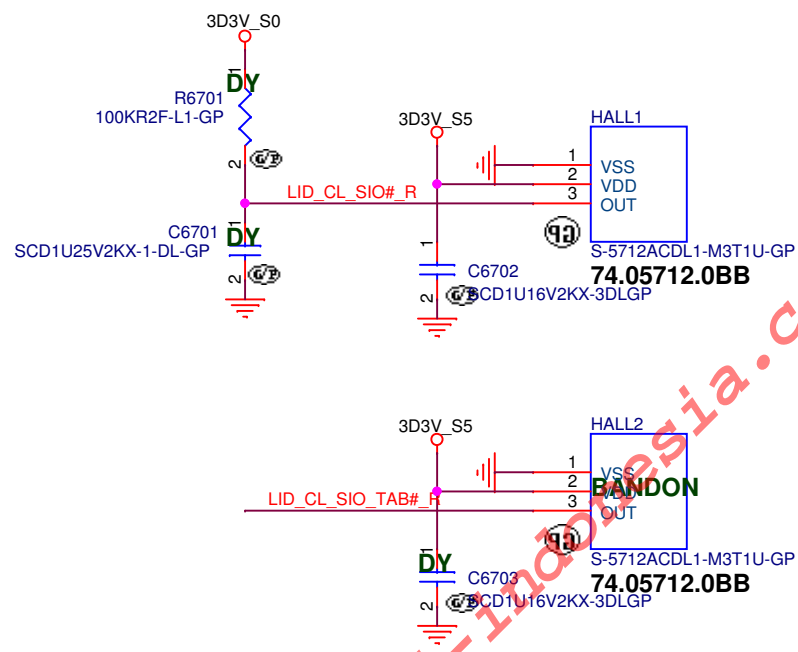
Date: Friday, February 15, 2019 Sheet 66 of 106

Main Func = Sensor (Hall-Sensor)

[24,55,64] LID_CL_SIO#_R << >>—
[24,64] LID_CL_SIO_TAB#_R << >>—


BANDON
TCS40DLR
[074.TCS40.M001]

NORTHBAY
APX8131A
[074.08131.007B]

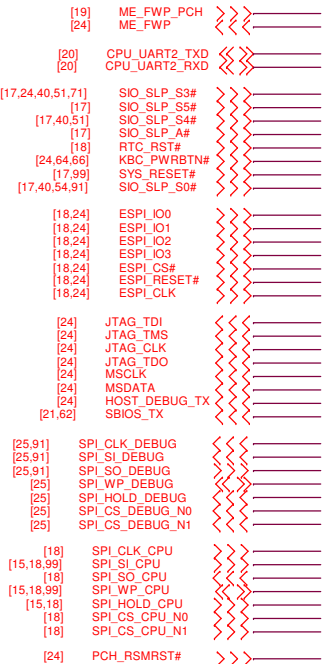


www.teknisi-indonesia.com

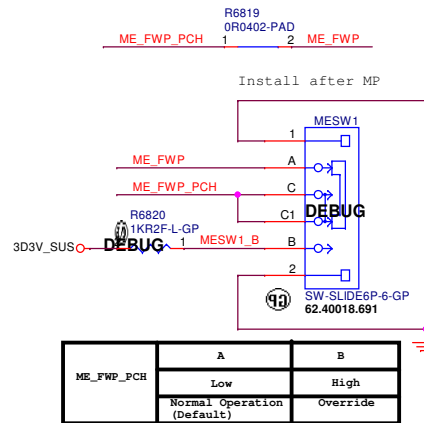
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Sensor (Hall-Sensor)					
Size A4	Document Number Bandon / NorthBay 13"				Rev X00
Date: Friday, February 15, 2019		Sheet 67		of 106	

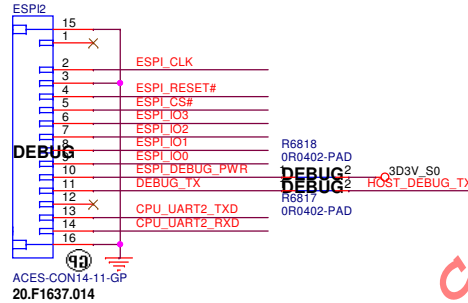
Main Func = Debug



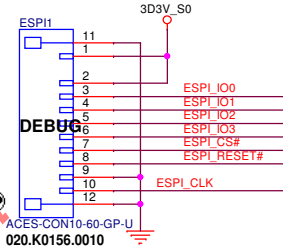
Firmware SW



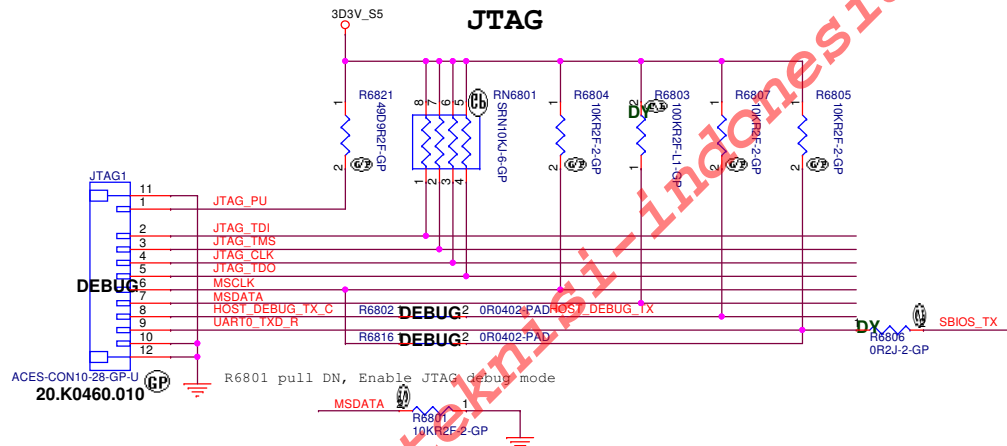
ESPI DEBUG (Wistron)



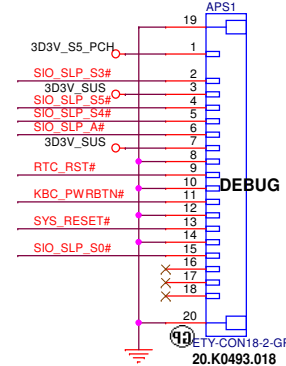
ESPI DEBUG (DELL)



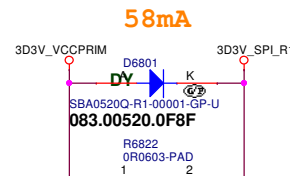
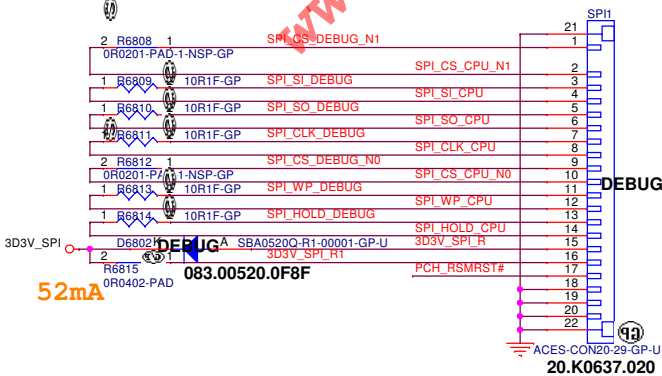
JTAG



APS DEBUG



SPI DEBUG



<Core Design>

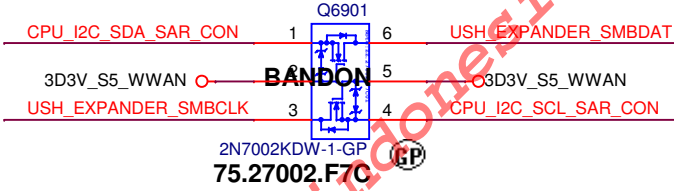
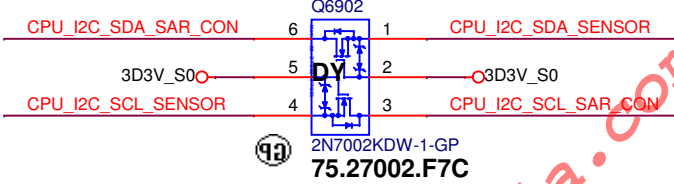
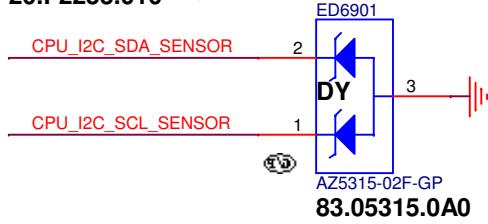
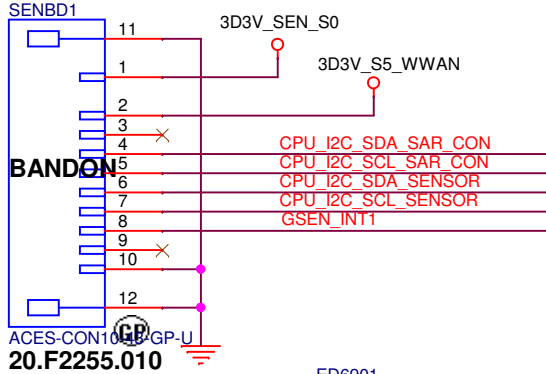
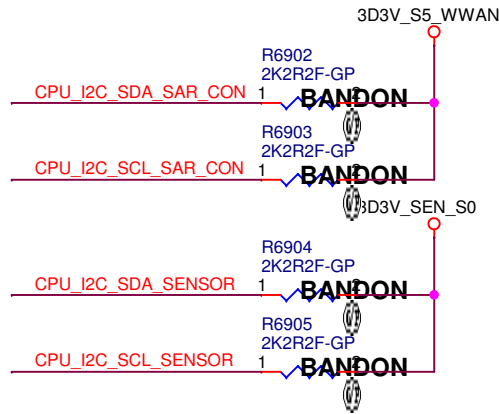
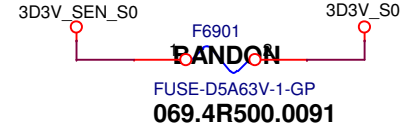
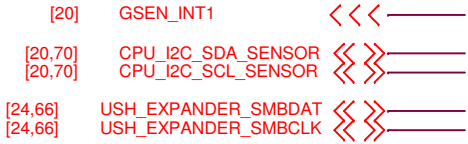
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Title **Debug (LPC debug)**

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Main Func = Sensor (E-compass/A+Gyro/SAR)



<Core Design>

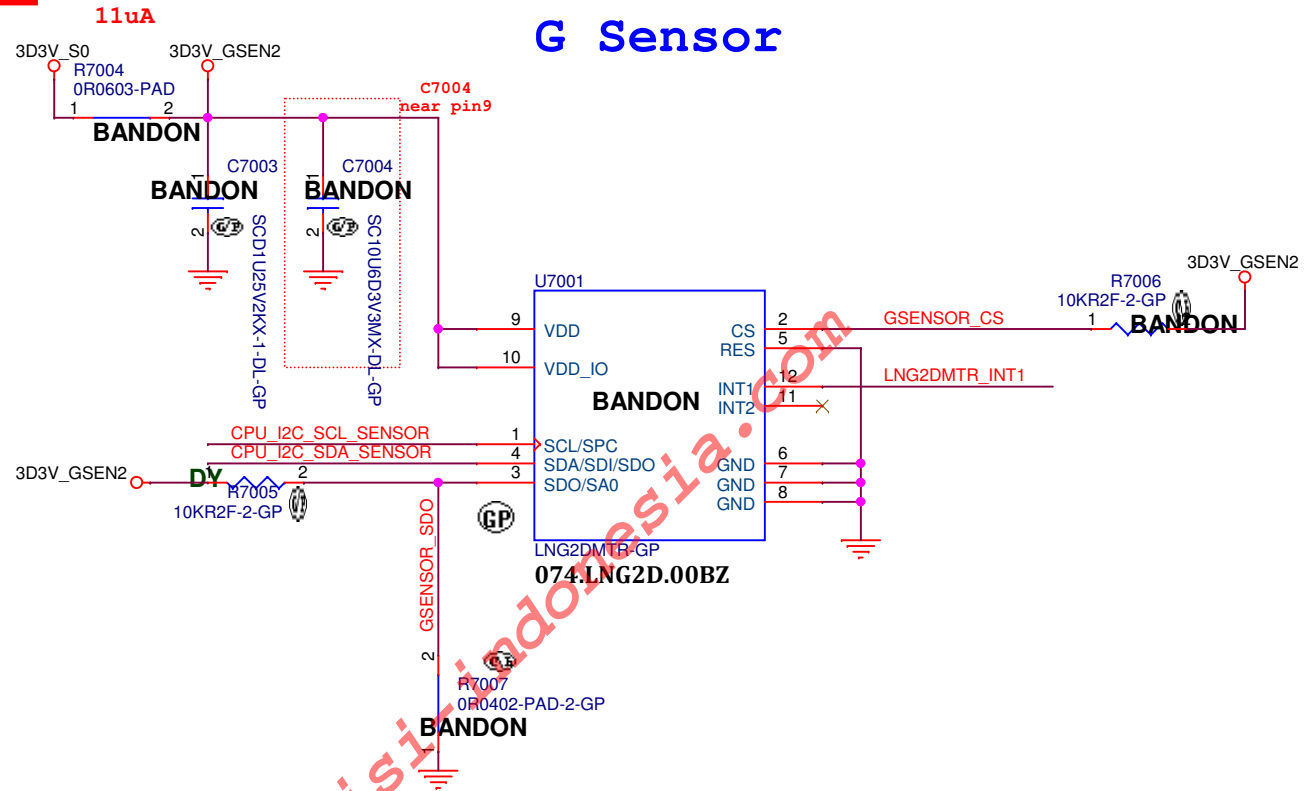
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Title
Sensor (GYROSCOPE/PRESSUE/ALS)

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Main Func = G-sensor

```
[20,69]    CPU_I2C_SDA_SENSOR  << >> _____
[20,69]    CPU_I2C_SCL_SENSOR  << >> _____
[20]       LNG2DMTR_INT1      << >> _____
```



<Core Design>



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Title

Sensor (G-sensor)

Size
A4

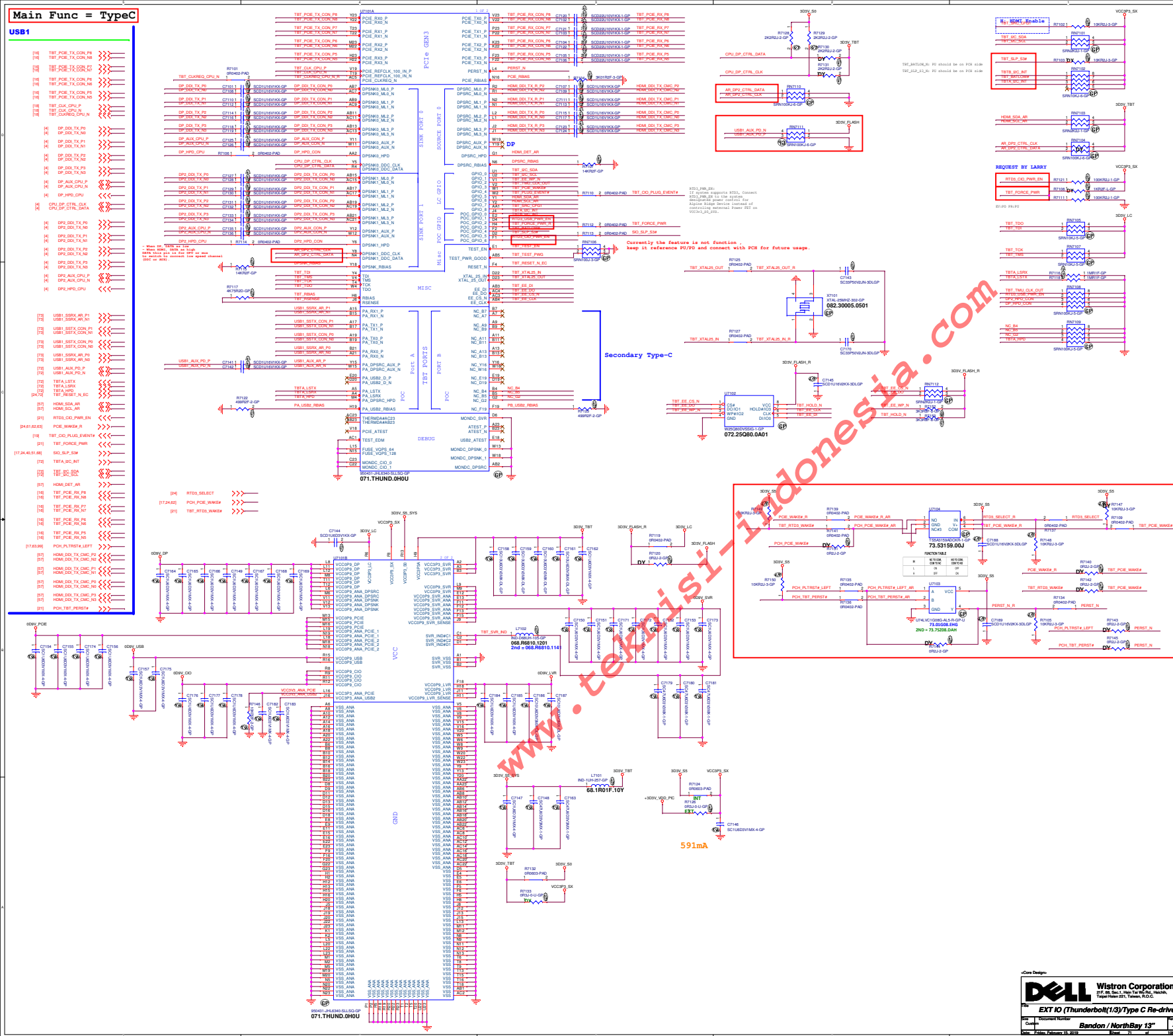
Document Number

Bandon / NorthBay 13"

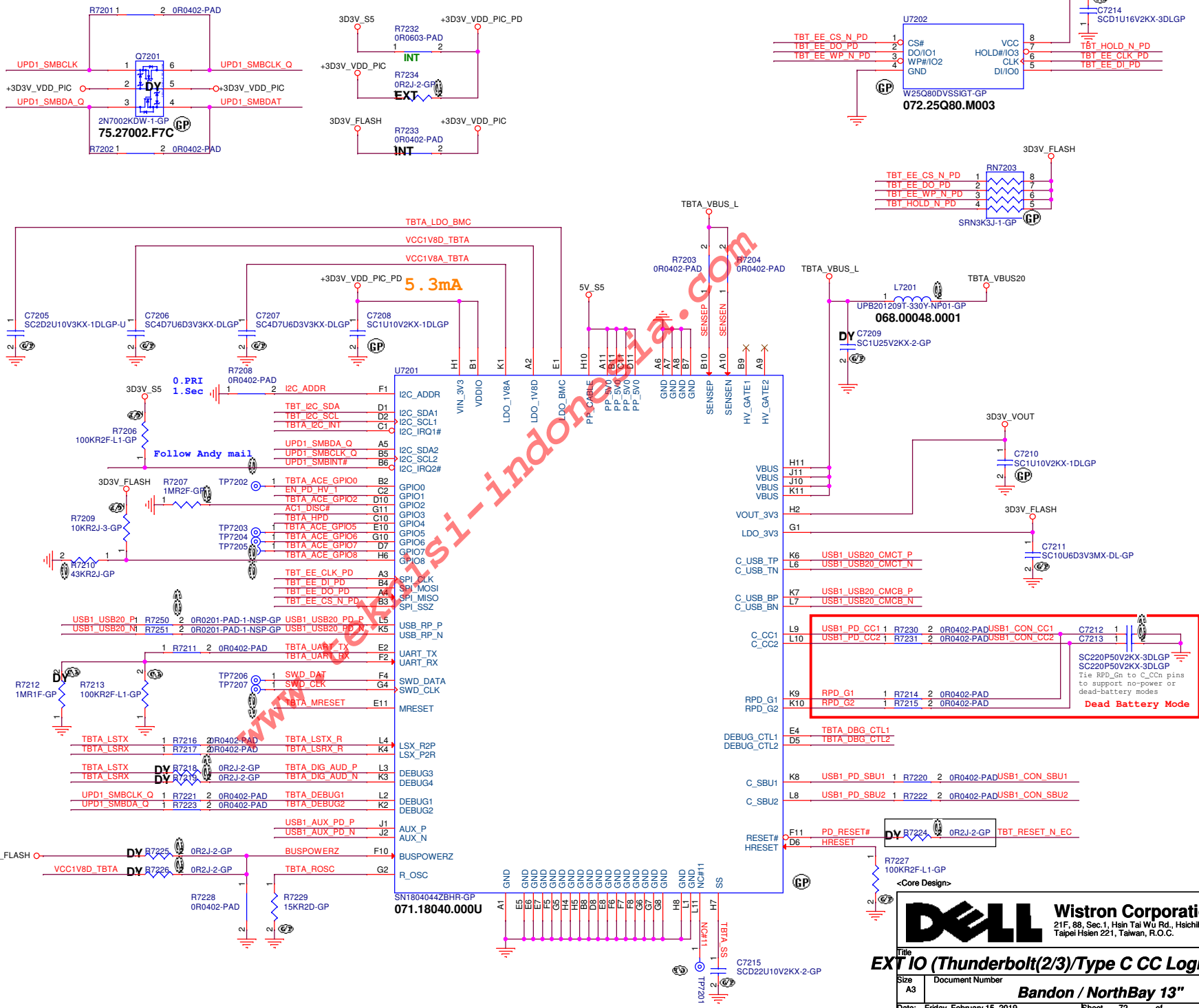
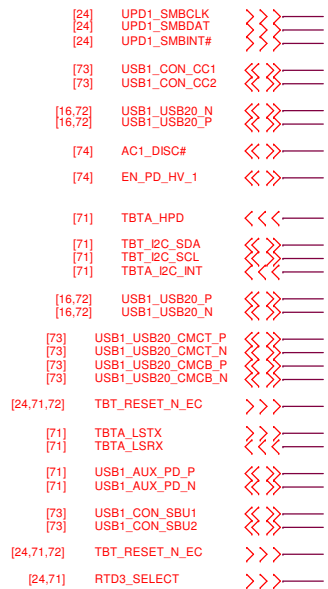
Rev
X00

Date: Friday, February 15, 2019

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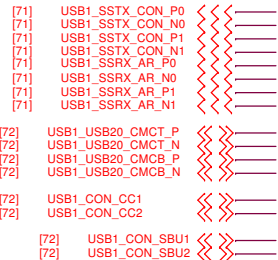


Main Func = TypeC

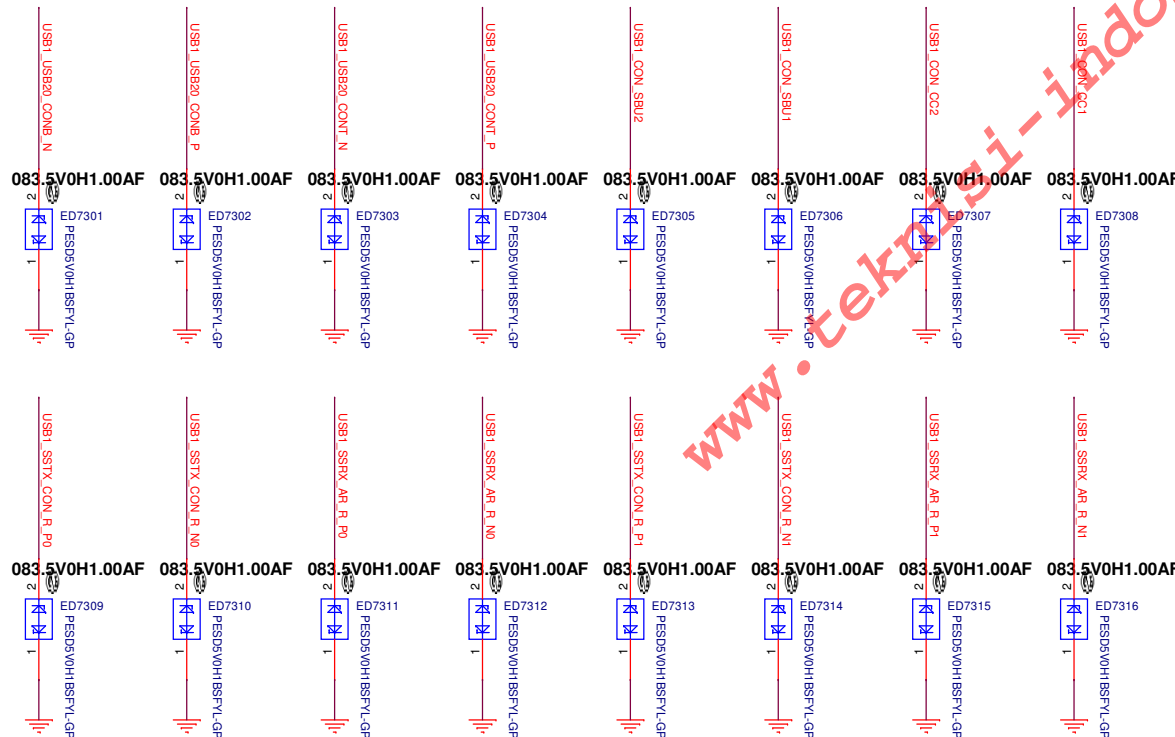
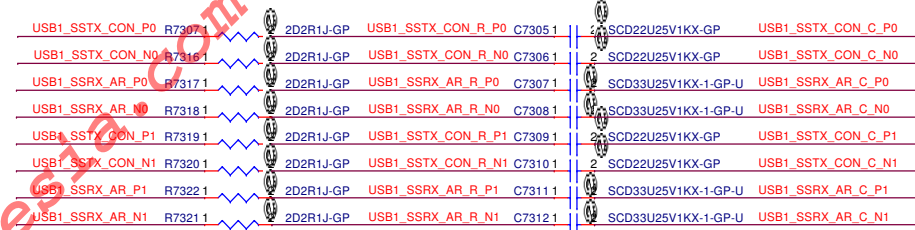
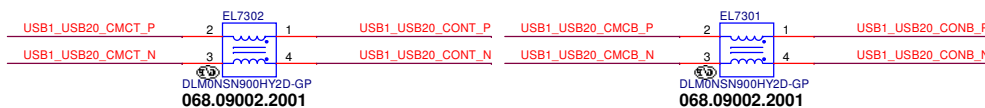
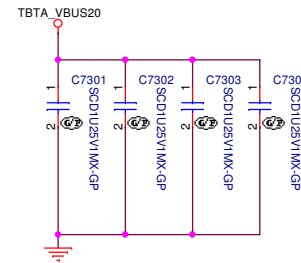
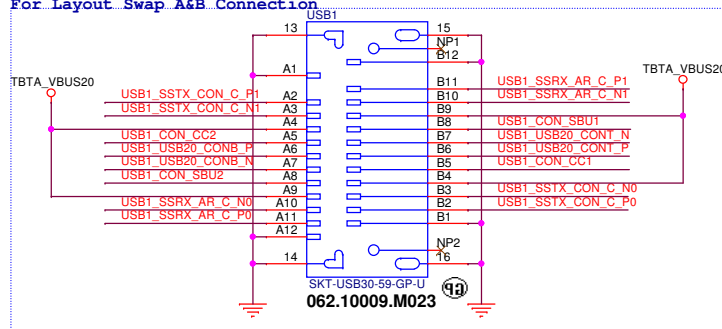


Main Func = TypeC

USB1



For Layout Swap A&B Connection



<Core Design>

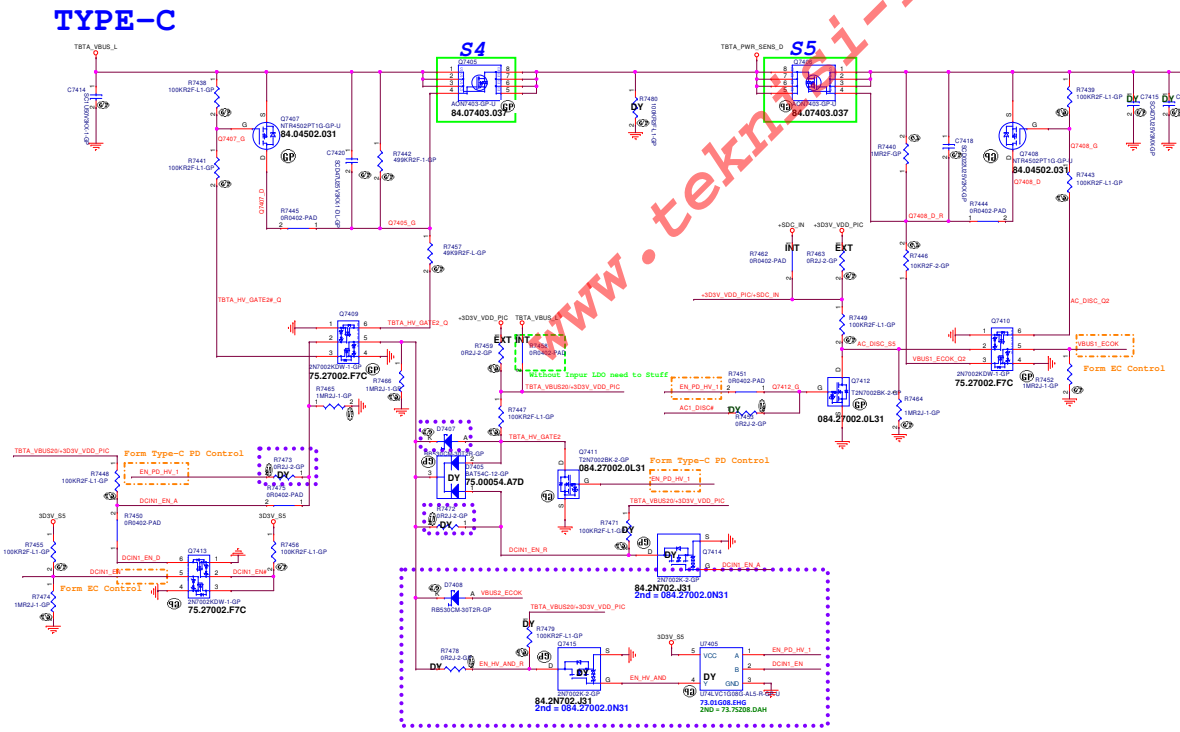
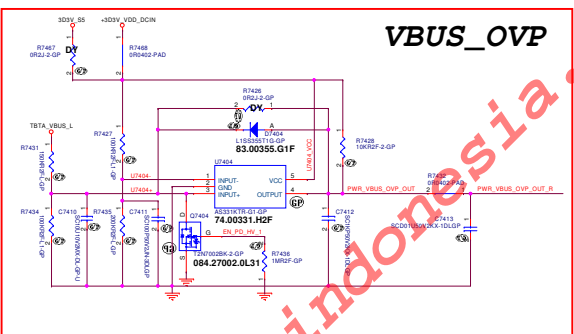
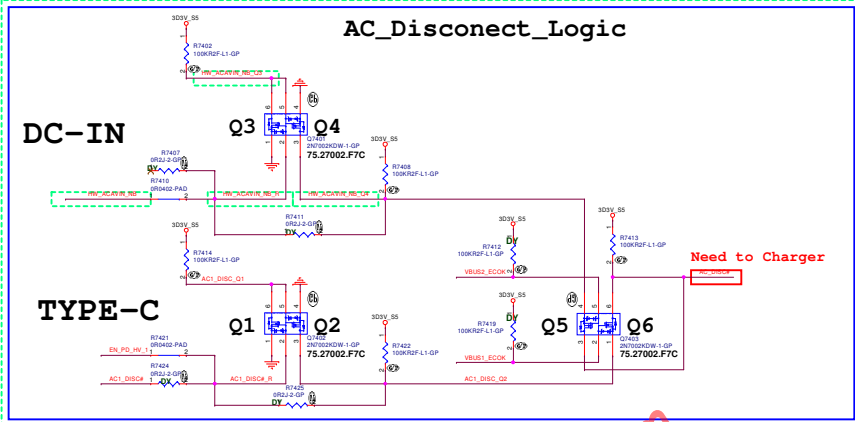
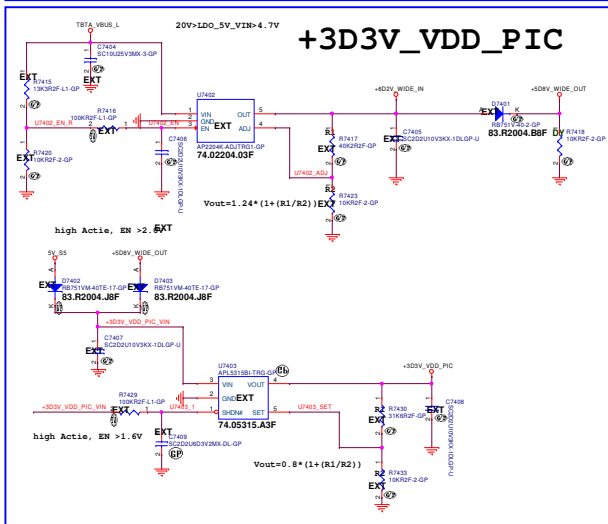
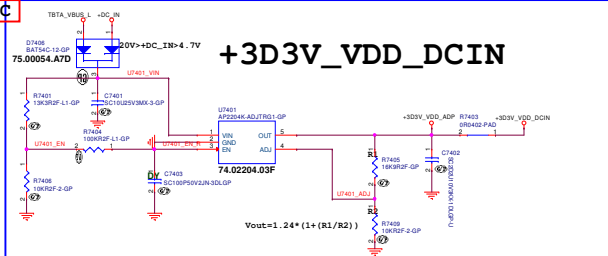
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Taipei Hsien 221, Taiwan, R.O.C.

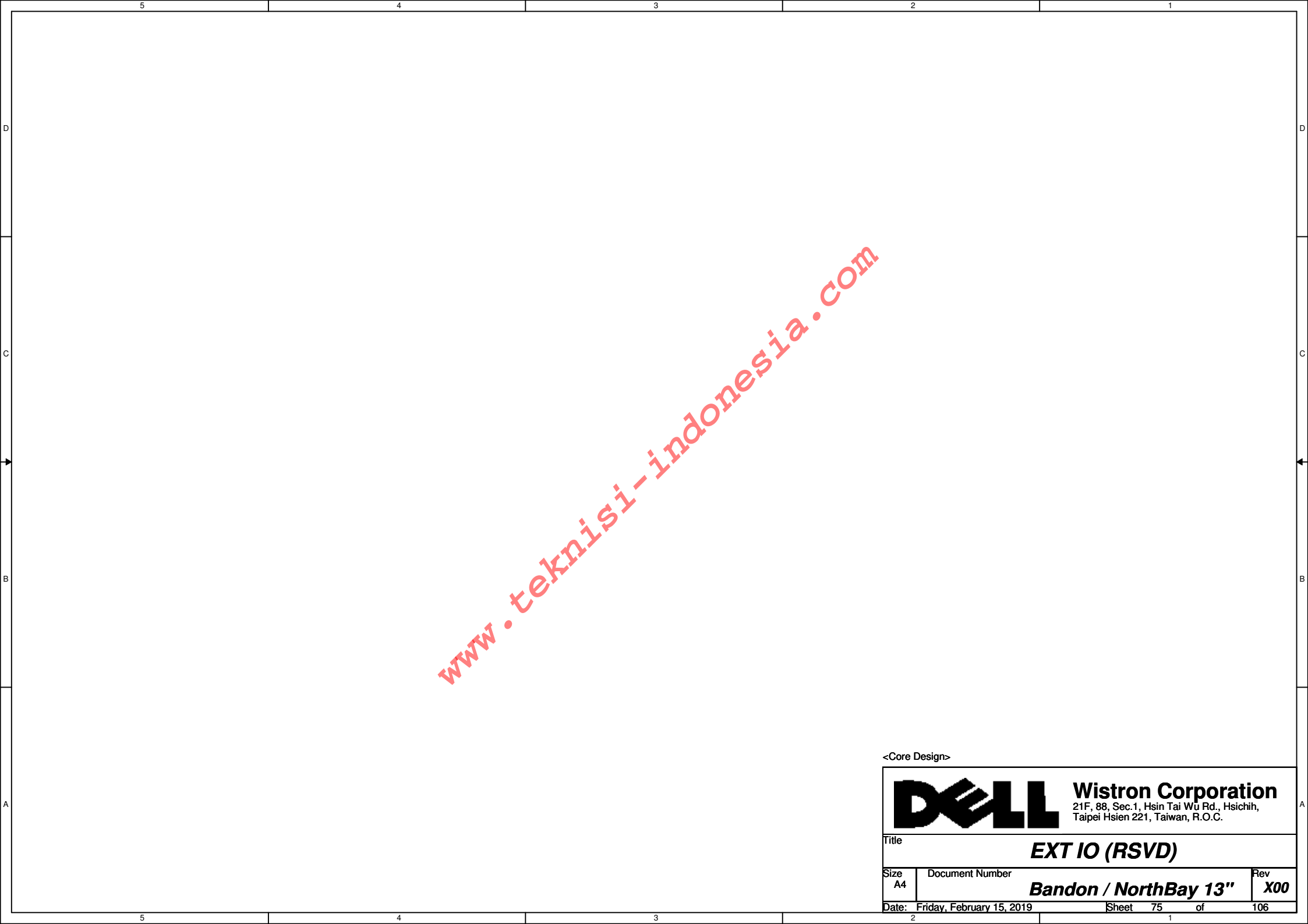
Title
EXT IO (Thunderbolt(3/3)/Type C Conn)

Size A3 Document Number **Bandon / NorthBay 13"** Rev **X00**

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[24,43,44]	HW_ACAVIN_NB	>>>
[72]	AC1_DISC#	>>>
[24,43]	VBUS1_ECOK	>>>
[72]	EN_PD_HW_1	>>>
[24,43]	AC_DISC#	>>>
[24]	DCIN1_EN	>>>
3]	PWR_VBUS_OVP_OUT_R	<<<
[24,44]	VBUS2_ECOK	>>>

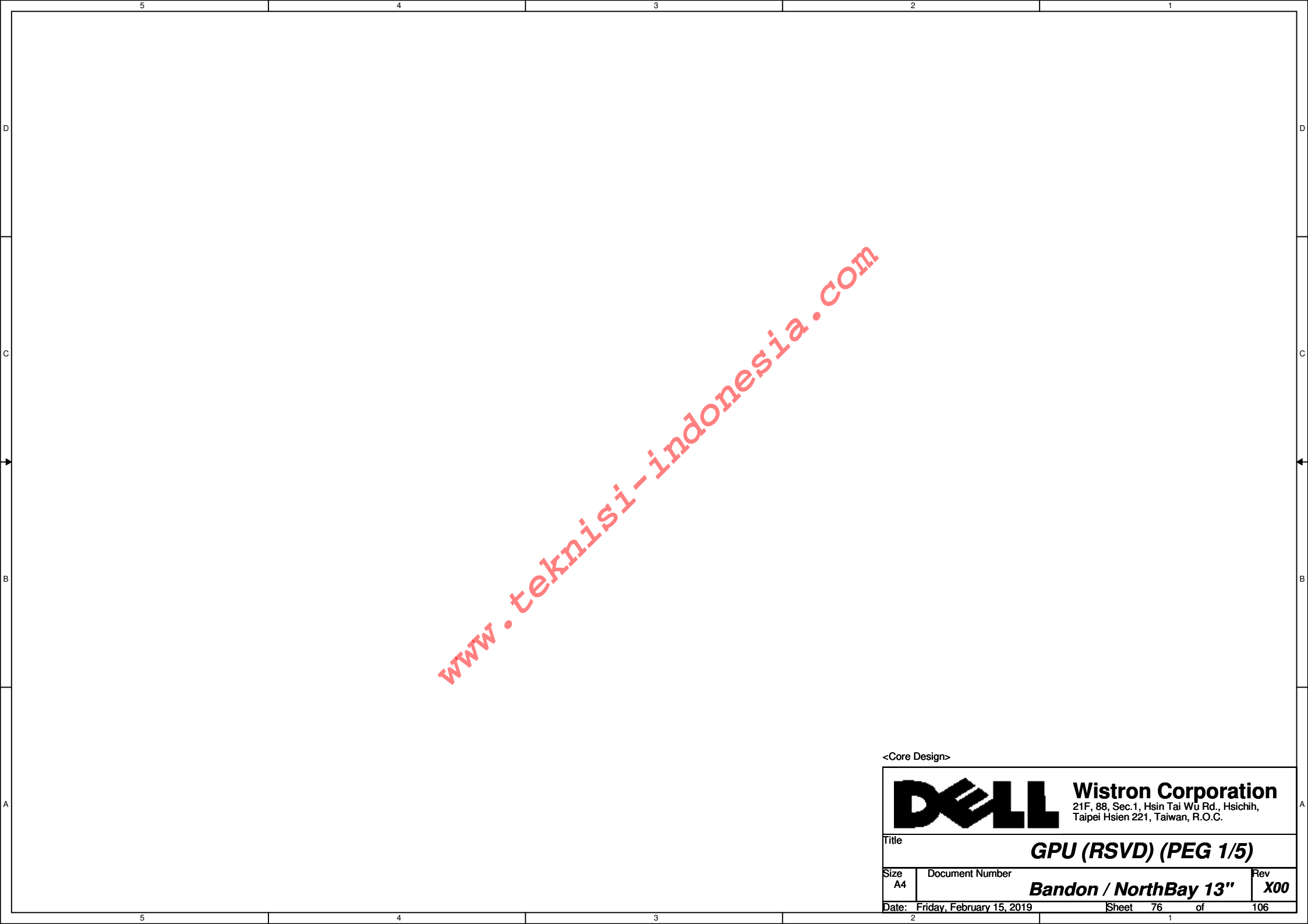




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Title EXT IO (RSVD)			
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title GPU (RSVD) (PEG 1/5)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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<Core Design>

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Title GPU (RSVD) (DIGITAL 2/5)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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Title GPU (RSVD) (VRAM 3/5)					
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Title GPU (RSVD) (GPIO 4/5)		
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<Core Design>

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Title GPU (RSVD) (PWR/GND 5/5)			
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title GPU (RSVD) (VRAM1,2 1/4)		
Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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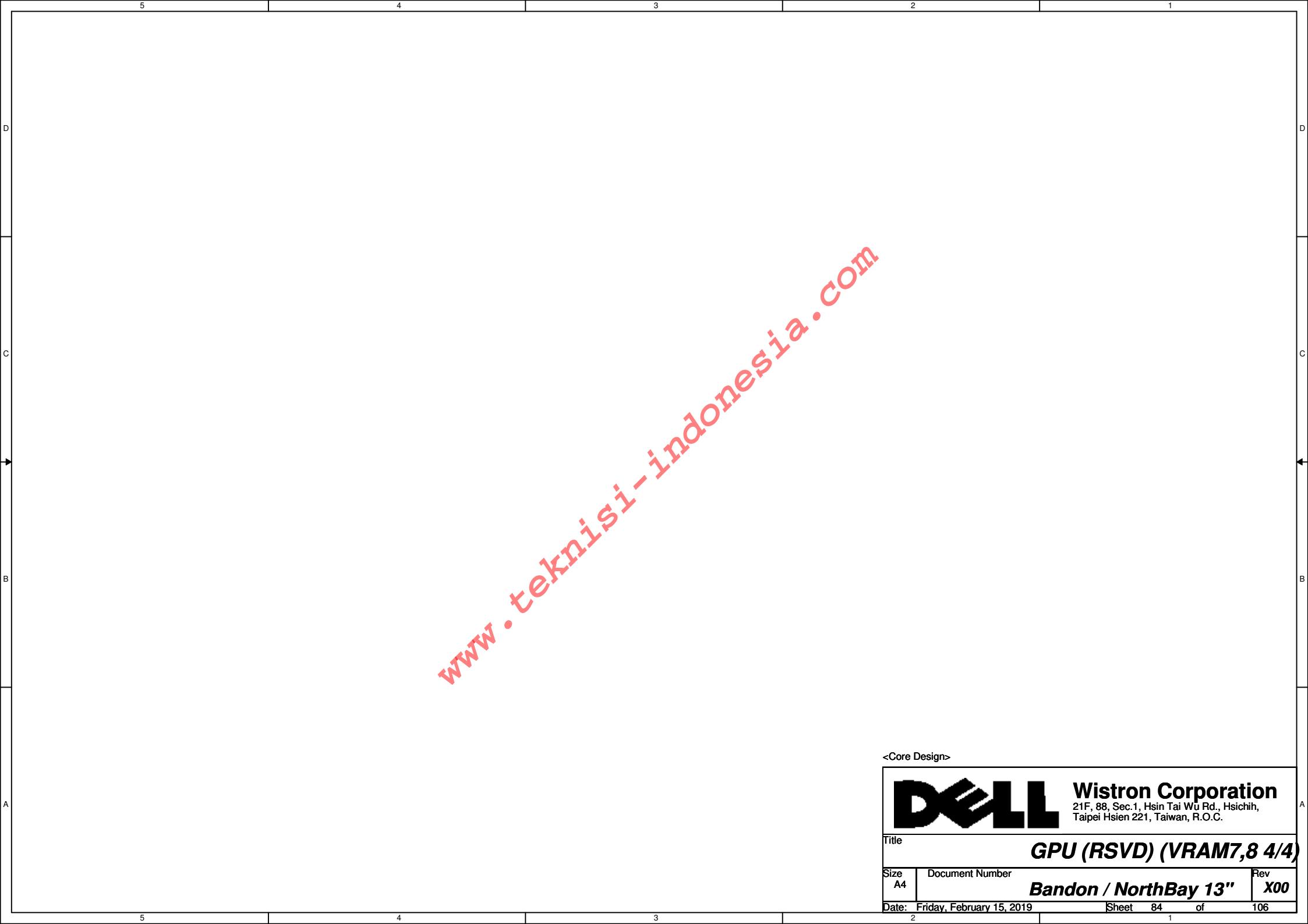
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Title GPU (RSVD) (VRAM3,4 2/4)		
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title GPU (RSVD) (VRAM5,6 3/4)					
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Title

GPU (RSVD) (VRAM7,8 4/4)

Size A4	Document Number Bandon / NorthBay 13"	Rev X00
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Title GPU (RSVD) (VGA_CORE)		
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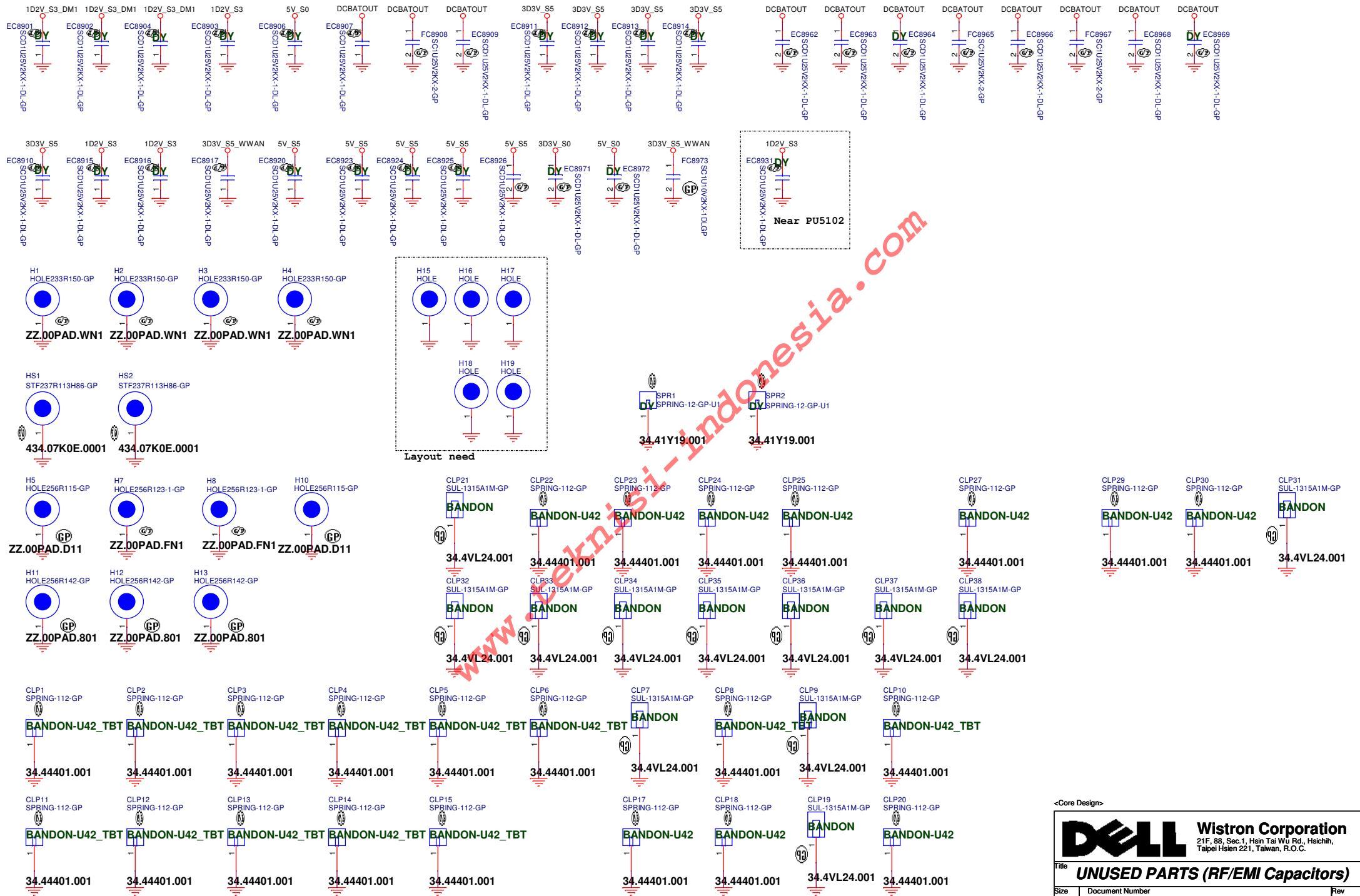
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Title GPU (RSVD)			
Size A4	Document Number Bandon / NorthBay 13"		Rev X00
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<Core Design>


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Title UNUSED PARTS (RSVD)			
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Main Func = EMC/ RF



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Title INT IO (RSVD) (NFC)			
Size A4	Document Number Bandon / NorthBay 13"		Rev X00
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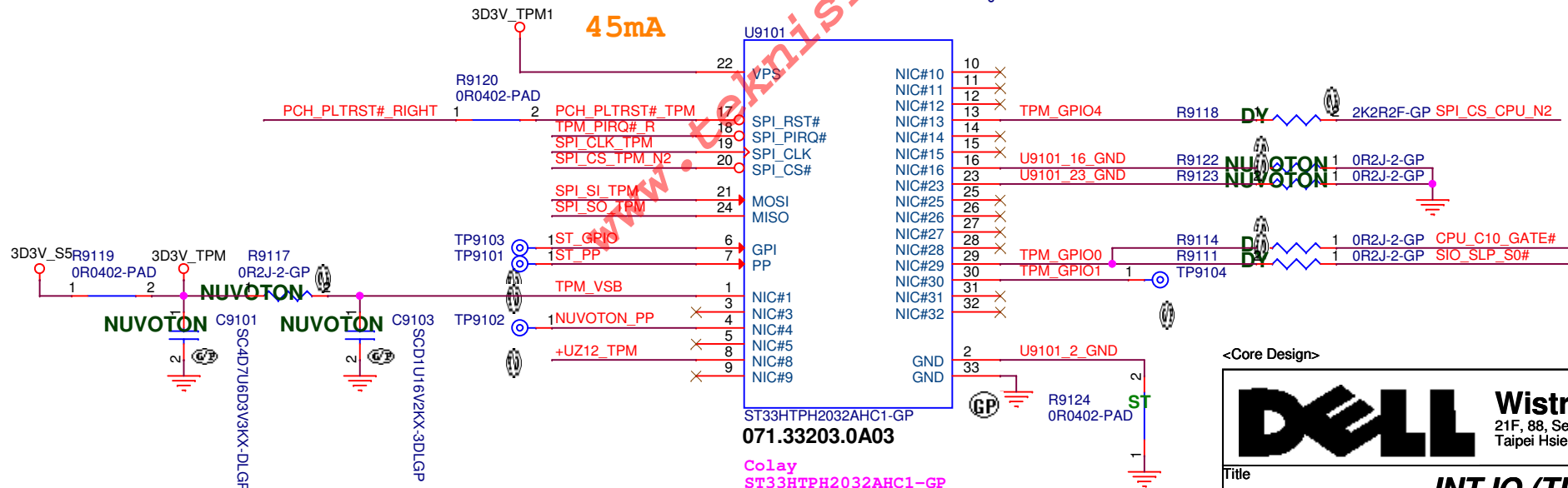
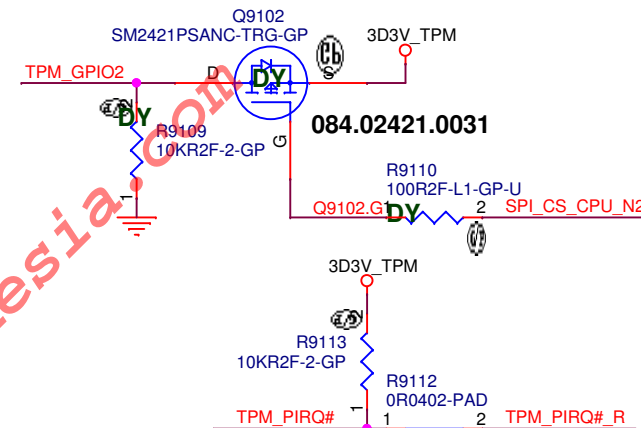
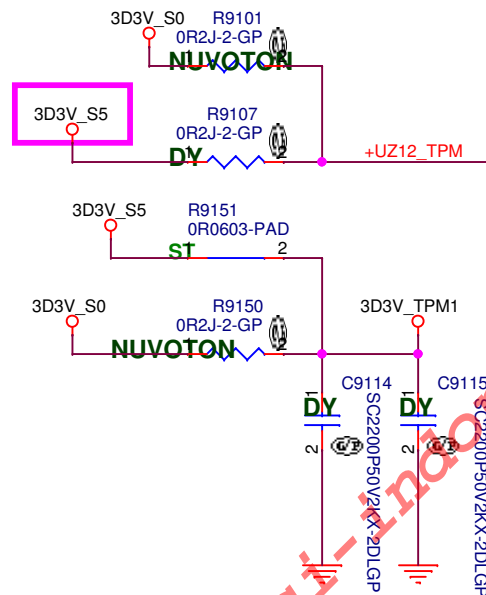
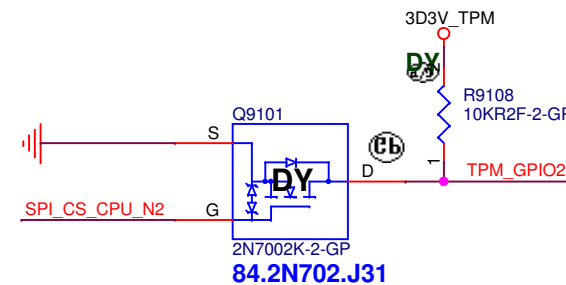
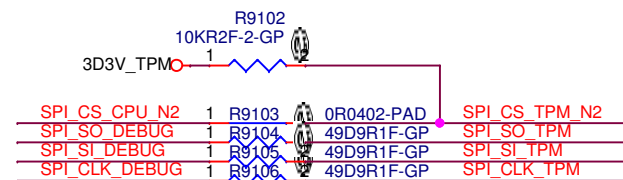
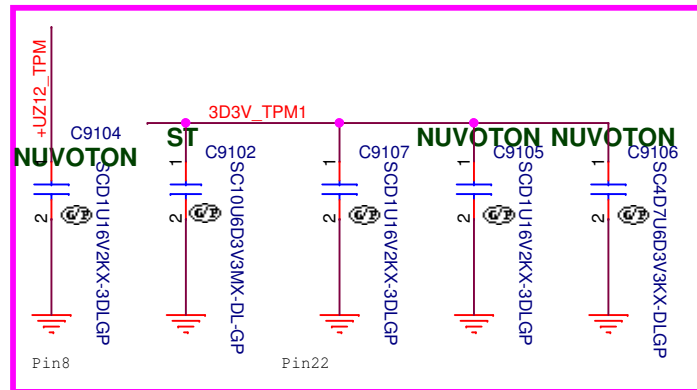
Main Func = TPM

[20] TPM_PIRQ#

[17,40,54,68] SIO_SLP_S0#

[17,33,61,62,97] PCH_PLTRST# RIGHT

[25,68]	SPI_CLK_DEBUG	~~~~~	_____
[25,68]	SPI_SI_DEBUG	~~~~~	_____
[25,68]	SPI_SO_DEBUG	~~~~~	_____
[18]	SPI_CS_CPU_N2	~~~~~	_____
[21,24,40,54]	CPU_C10_GATE#	~~~~~	_____



ST33HTPH2032AHC1-GP
071.33203.0A03

Colay
ST33HTPH2032AHC1-GP
071.33203.0A03
NPCT750JAAYX-1-GP
071.00750.M001

<Core Design>



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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	321-328
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-130
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-574
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-685

INT 10 (TPM)

Size

Document Number

Bandon / NorthBay 13"

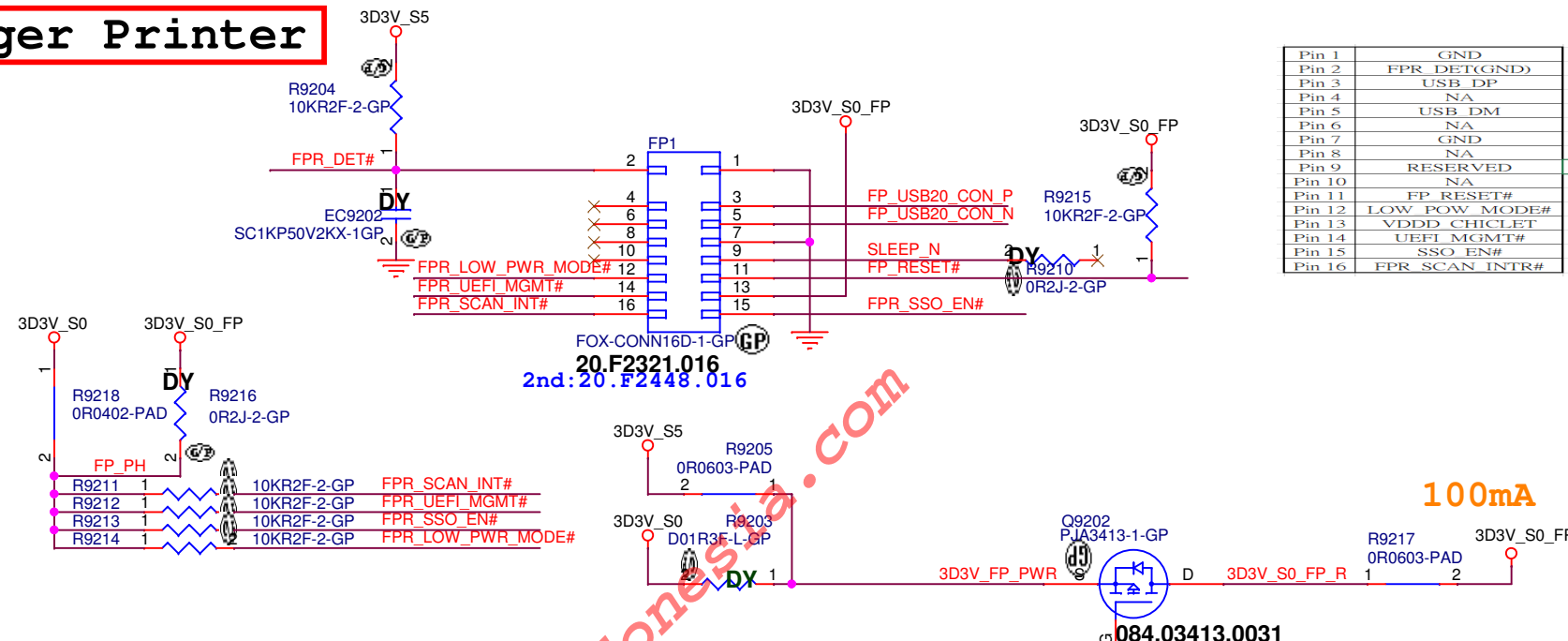
Rev	X00
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Main Func = Finger Printer

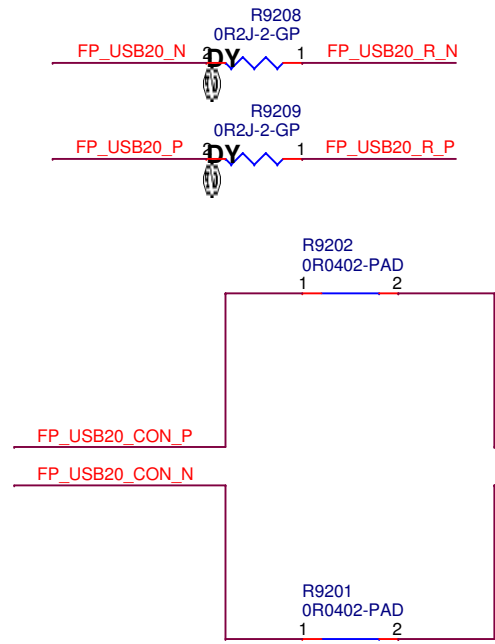
- [16] FP_USB20_N
- [16] FP_USB20_P
- [24,64] FPR_DET#
- [66] FP_USB20_USH_N
- [66] FP_USB20_USH_P
- [24] FPR_PWR_EN#
- [24,66] FPR_SCAN_INT#
- [24] FPR_SSO_EN#
- [24] FPR_UEFI_MGMT#
- [24] FPR_LOW_PWR_MODE#
- [66] FP_RESET#



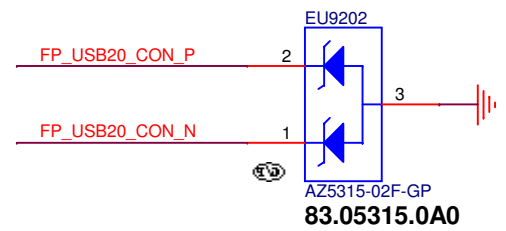
Pin 1	GND
Pin 2	FPR_DET(GND)
Pin 3	USB_DP
Pin 4	NA
Pin 5	USB_DM
Pin 6	NA
Pin 7	GND
Pin 8	NA
Pin 9	RESERVED
Pin 10	NA
Pin 11	FP_RESET#
Pin 12	LOW POW MODE#
Pin 13	VDD CHICLET
Pin 14	UEFI_MGMT#
Pin 15	SSO_EN#
Pin 16	FPR_SCAN_INTR#

PCH

USH



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Title**INT IO (Finger Printer)**

Size A4Document Number**Bandon / NorthBay 13"**Rev**X00**

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title EXT IO (RSVD) (Express Card/PCIE slot)		
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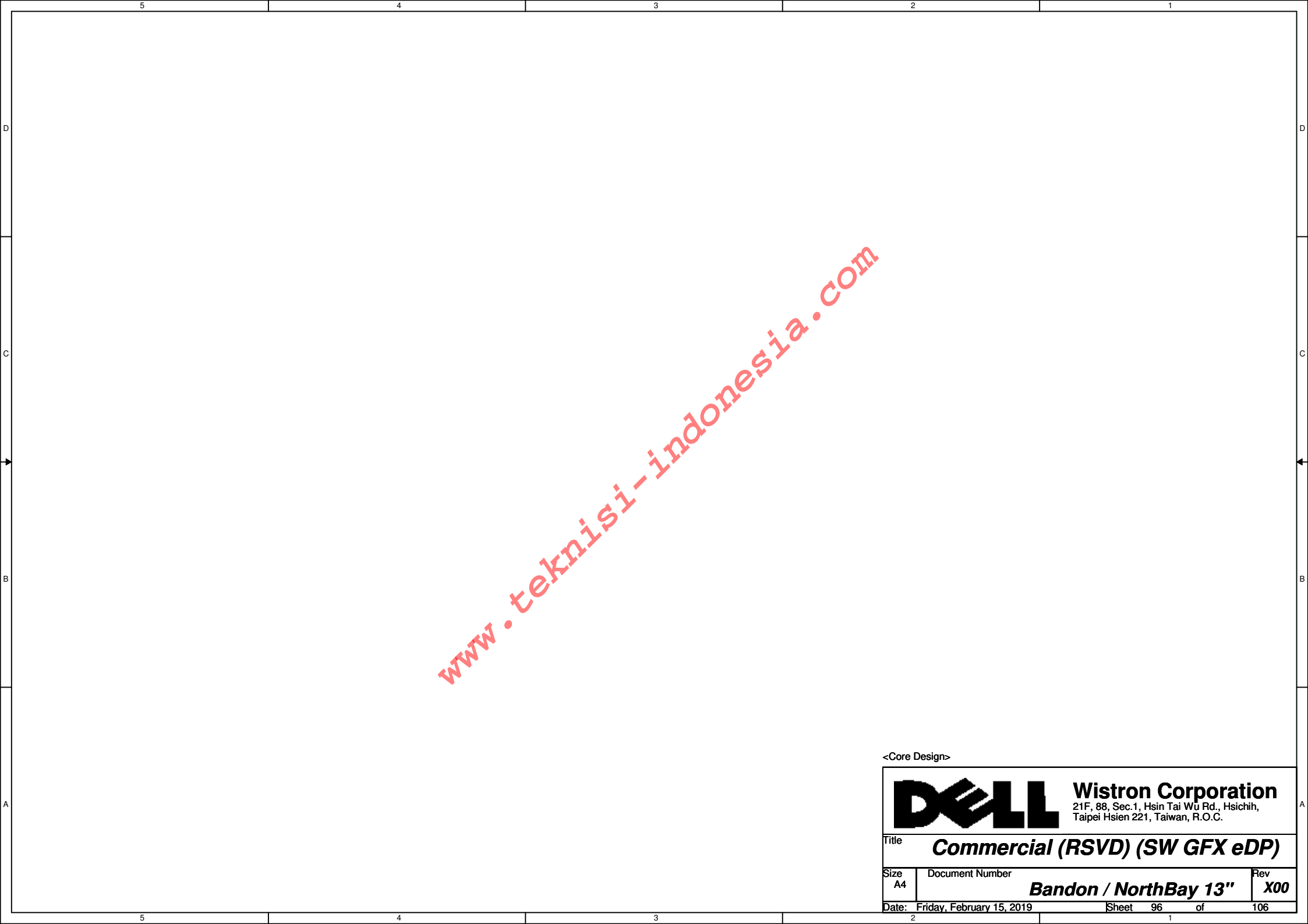
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title EXT IO (RSVD) (Smart Card/COM/PS2)					
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<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title EXT IO (RSVD) (Docking/LPT)					
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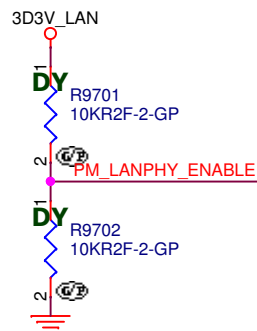


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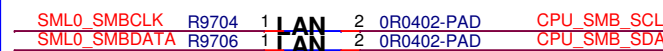
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Title Commercial (RSVD) (SW GFX eDP)					
Size A4		Document Number Bandon / NorthBay 13"			Rev X00
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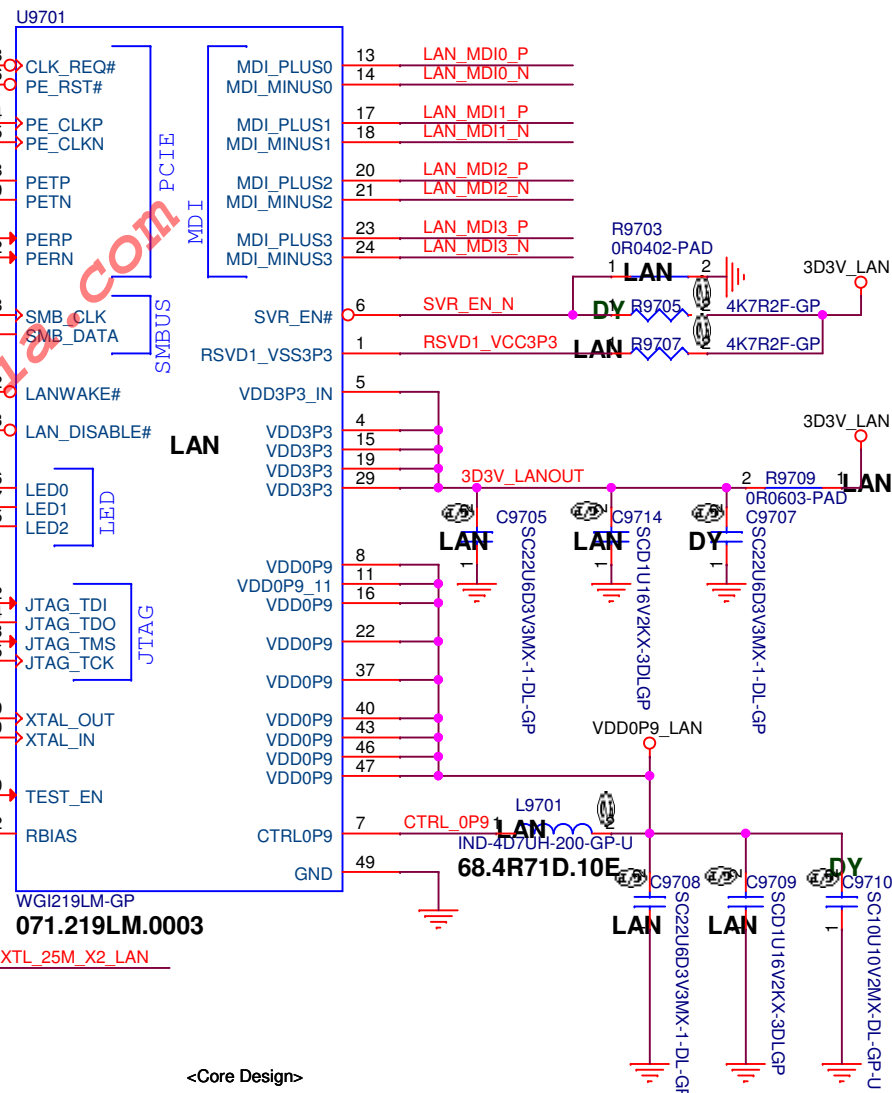
LAN



LAN_PCIE_RX_P	C9701	LAN_PCIE_RX_C_P
LAN_PCIE_RX_N	C9702	LAN_PCIE_RX_C_N
LAN_PCIE_TX_P	C9703	LAN_PCIE_TX_C_P
LAN_PCIE_TX_N	C9704	LAN_PCIE_TX_C_N



NOTE:DESIGN NOTE: LANWAKE_N must be connected to PCH's LANWAKE input.



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Commercial (Intel LAN)

Bandon / NorthBay 13"

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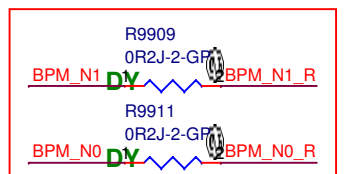
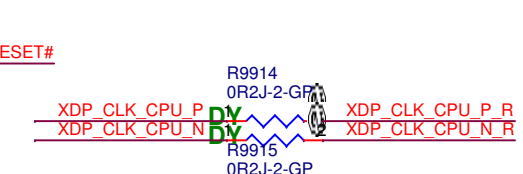
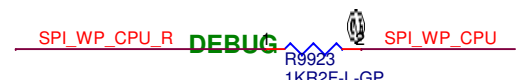
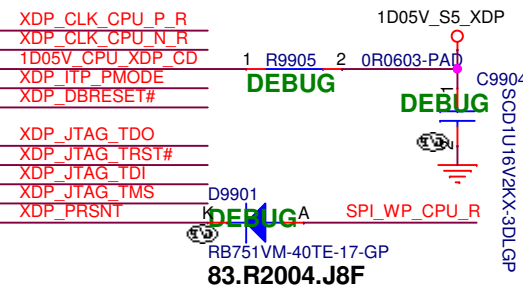
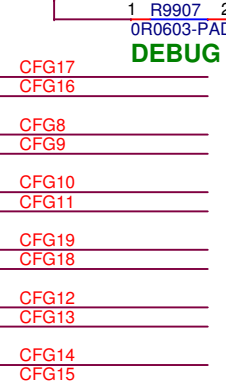
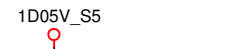
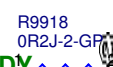
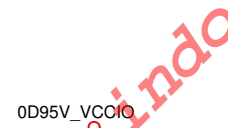
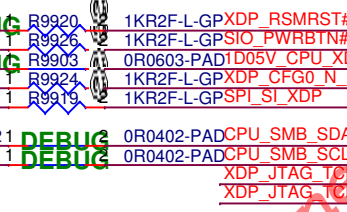
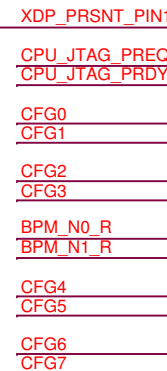
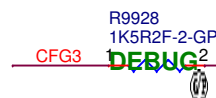
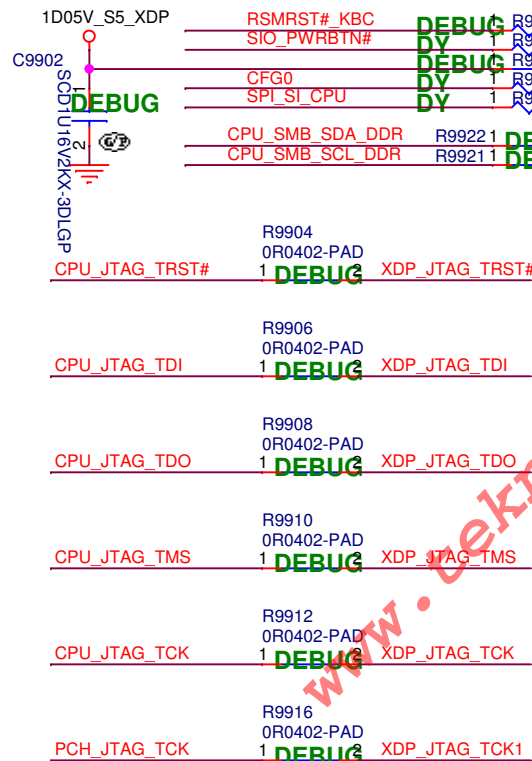
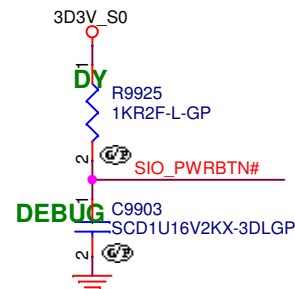
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Title Commercial (LAN Switch)					
Size A4	Document Number Bandon / NorthBay 13"				Rev X00
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Main Func = Debug (MIPI)

[6] CFG0 >>>—
[6] CFG1 >>>—
[6] CFG2 >>>—
[6] CFG3 >>>—
[6] CFG4 >>>—
[6] CFG5 >>>—
[6] CFG6 >>>—
[6] CFG7 >>>—
[6] CFG8 >>>—
[6] CFG9 >>>—
[6] CFG10 >>>—
[6] CFG11 >>>—
[6] CFG12 >>>—
[6] CFG13 >>>—
[6] CFG14 >>>—
[6] CFG15 >>>—
[6] CFG16 >>>—
[6] CFG17 >>>—
[6] CFG18 >>>—
[6] CFG19 >>>—
[3] BPM_N0 >>>—
[3] BPM_N1 >>>—
[6,15] ITP_PMODE >>>—
[18] XDP_CLK_CPU_N <<<—
[18] XDP_CLK_CPU_P <<<—
[3] PCH_JTAG_TCK <<<—
[3] CPU_JTAG_PRDY# <<<—
[3] CPU_JTAG_PREQ# <<<—
[3] CPU_JTAG_TRST# <<<—
[3] CPU_JTAG_TCK <<<—
[3] CPU_JTAG_TDI <<<—
[3] CPU_JTAG_TDO <<<—
[3] CPU_JTAG_TMS <<<—
[17,68] SYS_RESET# >>>—
[17,24] SIO_PWRBTN# >>>—
[12,13,18] CPU_SMB_SCL_DDR <<<—
[12,13,18] CPU_SMB_SDA_DDR <<<—
[17,63,71] PCH_PLTRST#_LEFT >>>—
[17,24,64] RSMRST#_KBC <<<—



<Core Design>



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Title			Debug (XDP debug)	
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Table of Content

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
 Capacitor type + value + rating + size + tolerance + material
 SCD1U10V2MX-1
 SC=> SMT Ceramic, TC=> POS cap or SP cap
 D1U => 0.1uF
 10V => the voltage rating is 10V
 2=> 0402, 3=>0603, 5=>0805
 M=>tolerance M, K, Z
 X=> X7R/X5R, Y=> Y5V
 -1 => symbol version, nonsense to EE characteristic

<Core Design>



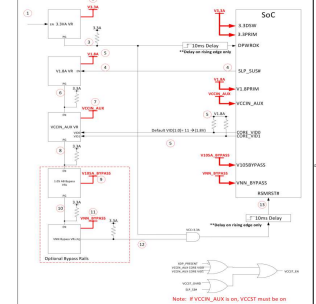
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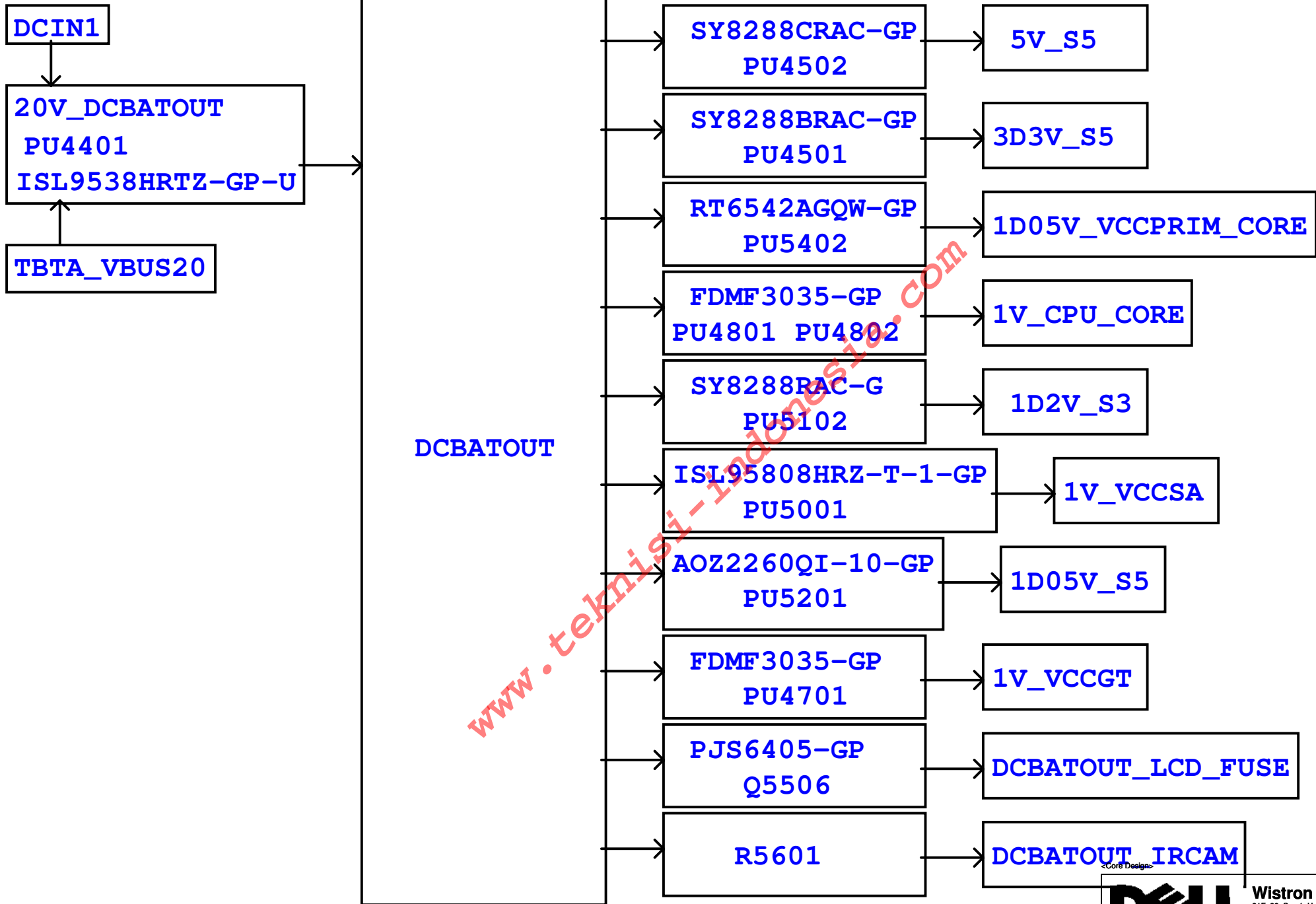
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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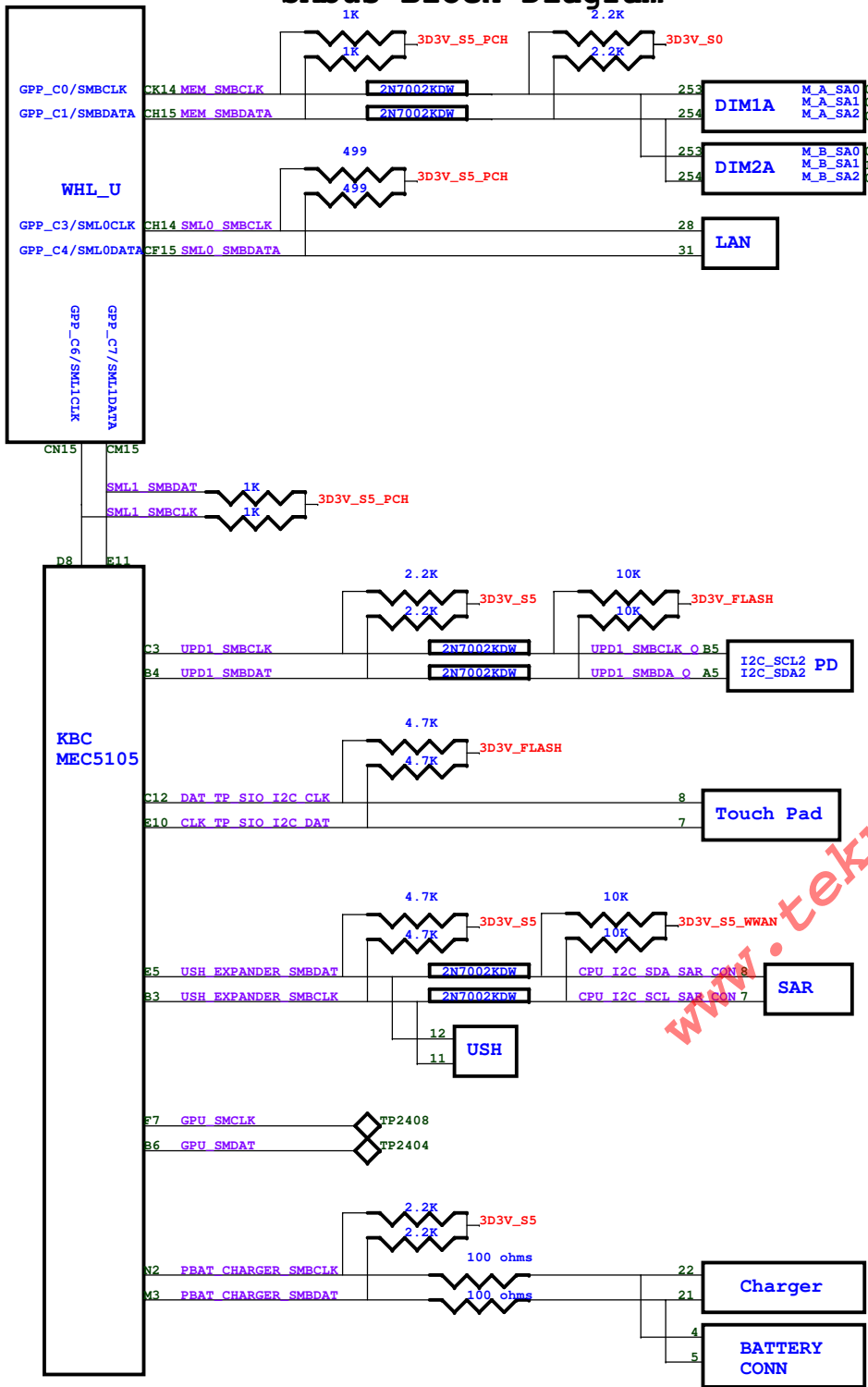
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ICL Non-DSx System Architecture Block Diagram





SMBus Block Diagram



I2C Block Diagram

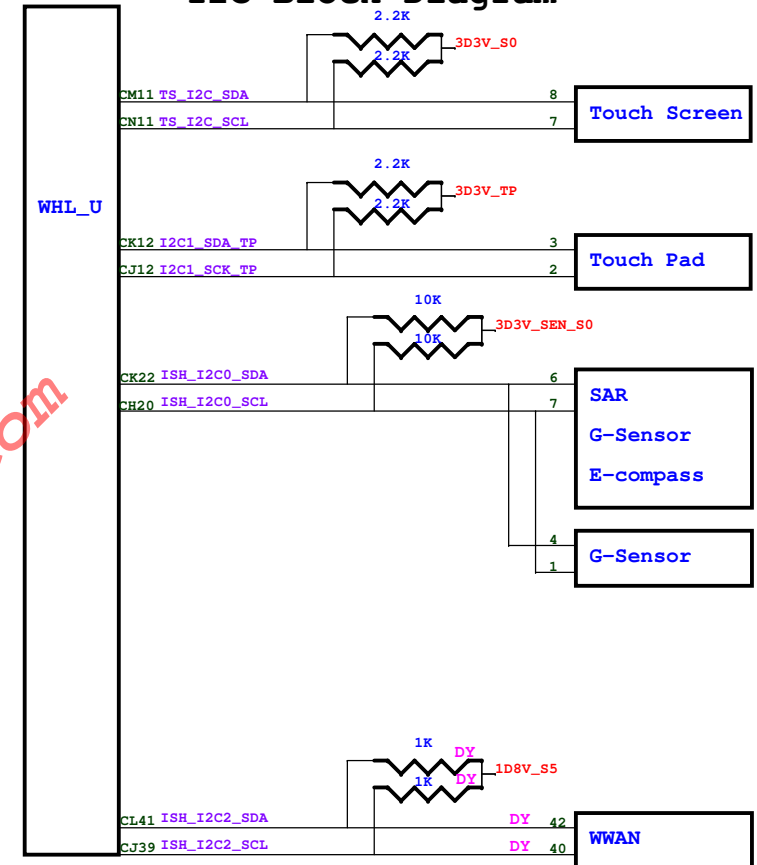


Table 6-103. Bus Capacitance/Pull-Up Resistor Relationship

Standard Mode (100kHz) - Pull-up / Pull-down Resistor Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength (Refer EDS)
Upto 400 pF	2.2KΩ	100Ω
Fast Mode (400kHz) - Mode Pull-up/ Pull-down Strength Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength

Upto 100pF	2.7KΩ	100Ω
Upto 200pF	1.5KΩ	
Upto 300pF	1KΩ	
Upto 400 pF	680Ω	
Fast mode Plus (1MHz) - Pull-up/Pull-down strength Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength
Upto 50pF	2.2KΩ	100Ω
Upto 100pF	1.2KΩ	
Upto 200pF	560Ω	
Upto 300pF	390Ω	
Upto 400 pF	270Ω	67Ω

LAN DATASHEET

Pin Name	Pin #	Type	Op Mode	Name and Function
SMB_CLK	28	O/d	Bi-dir	SMBus clock. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499Ω resistor (while in Sx mode).
SMB_DATA	31	O/d	Bi-dir	SMBus data. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499Ω resistor (while in Sx mode).

<Core Design>

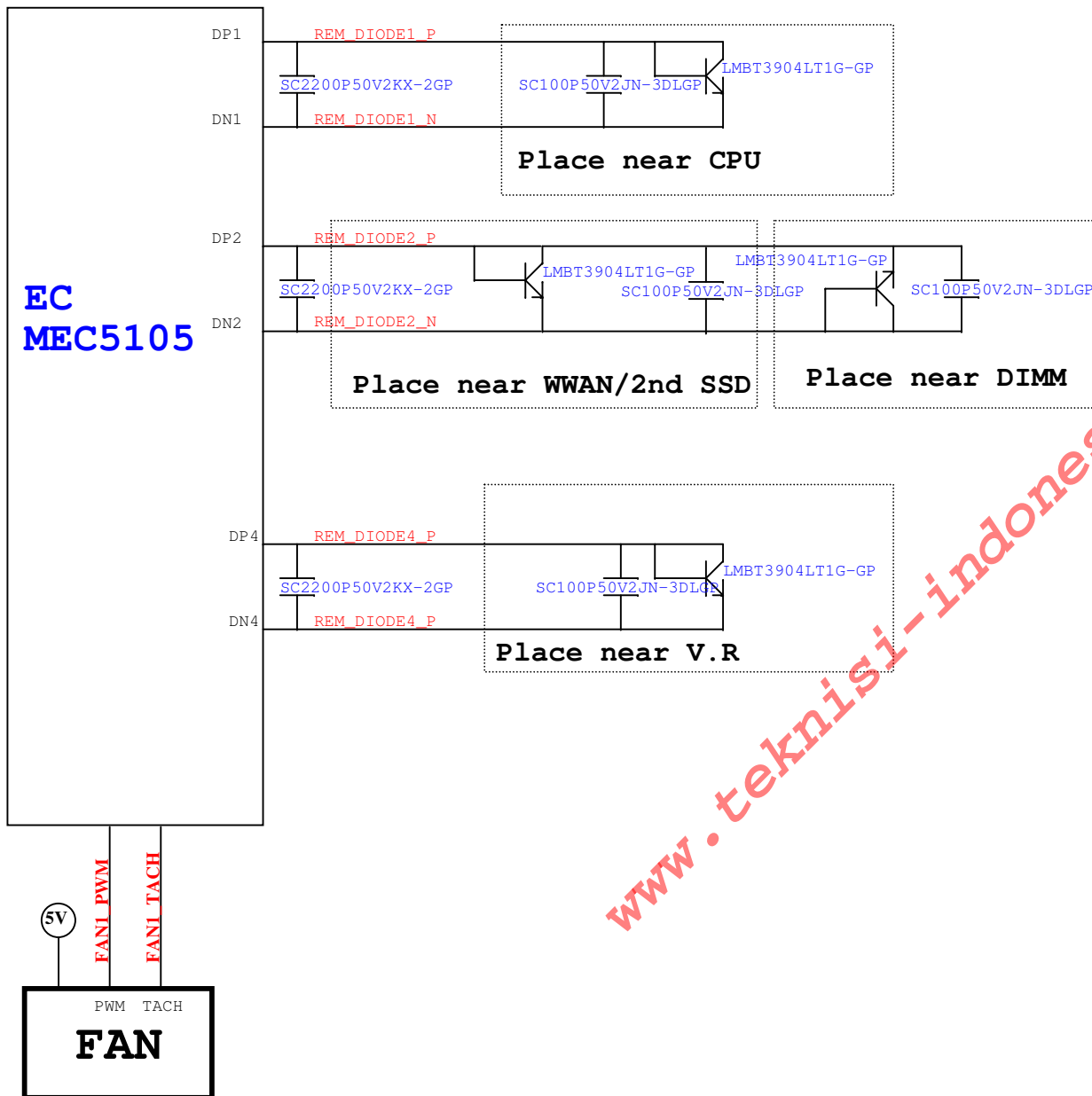
DELL Wistron Corporation
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Title **SMBUS/I2C BLOCK DIAGRAM**

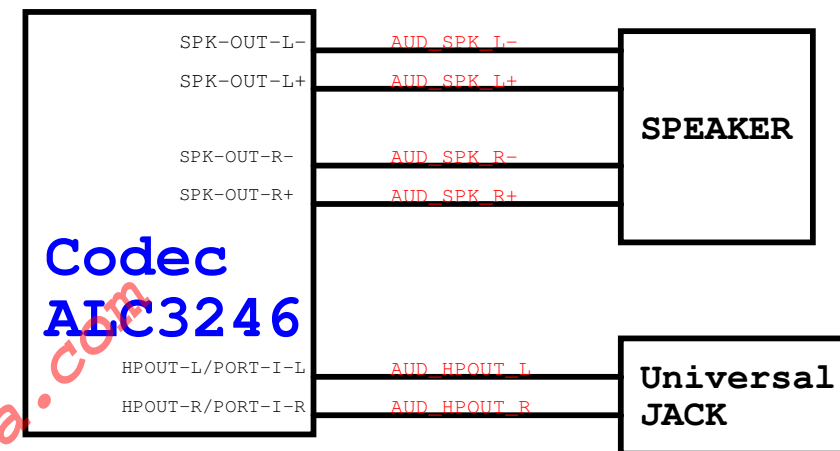
Size A3 Document Number **Bandon / NorthBay 13"** Rev **X00**

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Thermal Block Diagram



Audio Block Diagram



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Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.


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